

ZZ-ES0AA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame B1 Sequence 207  
: P1W124.MCR 600,1204] MICRO2 1L(03) i4-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 206  
: FORKS .MIC [600,1204] I-stream decode forks : A-FORK for VAX Instructions

B 1

:7533 ;HERE FOR CLRQ=CLRD  
:7534  
:7535 04D: -----  
U 004D, 0018,0C38,1980,F980,0000,004F :7536 CLRQ: RCET0]\_K[ZERO] ;CLRQ/CLRD - MAKE TWO LONGWORDS OF ZERO  
:7537  
:7538 ;HERE FOR CLRx, x=B, W, L (CLRF=CLRL)  
:7539  
:7540 04F: -----  
U 004F, FF18,0038,19F0,F847,0000,0200 :7541 CLR: ALU\_K[ZERO],D\_0, ;SETUP ZERO TO STORE  
:7542 B.FORK ;GO STORE IT  
:7543  
:7544 ;HERE FOR MOVPSL  
:7545  
:7546 04E: -----  
U 004E, 0000,003C,3DF0,2C00,0000,0089 :7547 MOVPSL: Q\_ID[PSL] ;READ PSL OVER ID BUS  
:7548  
:7549  
:7550 WRQ.DST:D\_Q, -----  
U 0089, FC00,003F,01F0,F847,0000,0300 :7551 WRITE.DEST,J/WRD ;MOVE TO D FOR STORAGE  
;STORE IT, DO NOT CHANGE CC

:7552 ;HERE ARE EXECUTION STATES FOR ESCAPES AND RESERVED INSTRUCTIONS  
 :7553  
 :7554 081: -----;RC[TO].K[.10].J/EXCPT ;ESCE - FAULT THROUGH 10  
 :7555  
 :7556  
 :7557 083: -----;RC[TO].K[.10].J/EXCPT ;ESCF - FAULT THROUGH 10  
 :7558  
 :7559  
 :7560 085: -----;RC[TO].K[.10].J/EXCPT ;ESCD - FAULT THROUGH 10  
 :7561  
 :7562  
 :7563 : \*\*\*\*\*  
 :7564 : \* Patch no. 070, PCS 0085 trapped to WCS 1180 \*  
 :7565 : \*\*\*\*\*  
 :7566  
 :7567 087: -----;RC[TO].K[.10].J/EXCPT ;RESERVED OPCODE - FAULT THROUGH 10  
 :7568  
 :7569  
 :7570 086: -----;RC[TO].K[.14].J/EXCPT ;ESCC - FAULT THROUGH 14  
 :7571  
 :7572  
 :7573 ;HERE FOR RSB  
 :7574  
 :7575 08A: -----;RSB: VA\_R[SP] ;ADDRESS OF TOP OF STACK  
 :7576  
 :7577  
 :7578  
 :7579 R[SP].LA+K[.4].RLOG, ;UPDATE STACK POINTER  
 :7580 D[LONG].CACHE, ;GET RETURN ADDR.  
 :7581 J/JMP ;JUMP TO IT  
 :7582  
 :7583 ;HERE FOR BREAKPOINT  
 :7584  
 :7585 08C: -----;BPT: RC[TO].K[.B0].RIGHT2, ;BREAKPOINT  
 :7586 J/EXCPT ;VECTOR ADDRESS IS 2C  
 :7587 ;TAKE THE FAULT  
 :7588  
 :7589 ;HERE IS NO OPERATION  
 :7590  
 :7591 08E: -----;NOP: L1.R.OPC ;DO NOTHING MUCH  
 :7592 P1.R.IRD  
 :7593  
 :7594  
 :7595 08F: -----;HALT: D.K1 ;DO EVEN LESS  
 :7596 PSL.MODE?,J/HALT.INST ;GO TELL CONSOLE WE HIT HALT INSTR  
 :7597

U 0200, 0C00,007F,15E0,BC00,0000,0300

U 0201, 0000,003C,0180,F800,0000,0001

U 0202, 0F01, 207F, 15E0, BD88, 0000, 0300

U 0203, 0000,003C,0180,F800,0000,0001

U 0204, 0800,007F,15E0,B00,0000,0300

U-0226 6001 6036 6120 5826 4670 6042

41-6205 0000 0036 0180 5800 0000 0001

D 1

I-stream decode for 14-Jan-82      Fiche 2 Frame D1      Sequel  
 (03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124

I-stream decode forks : B-FORK for VAX Instructions

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7598 .TOC      "      I-stream decode forks : B-FORK for VAX Instructions"
7599
7600 ;Control passes to this point from any 'B.FORK' state.
7601 ;The state of the data path is :
7602   LA, LB = Register selected by bits <3:0> of IB byte 1
7603   VA    = Address of first operand
7604   D     = First operand
7605   Q     = Instruction stream data, if any
7606   PC    = Address of next specifier
7607
7608 200: -----
7609 B.FORK: Q,D,D,Q,          ;S^# SHORT LITERAL
7610      ID,D,SYNC,          ;SEND FIRST OP OUT FOR ACCEL
7611      C.FORK
7612
7613 201: -----
7614      J/R SVMOD           ;RESERVED MODE
7615
7616 202: -----
7617      RC[T1],Q,            ;QUAD/DOUBLE. PUT FIRST WORD
7618      ID,D,SYNC,          ;SEND FIRST OP OUT FOR ACCEL
7619      Q,D,D,0,            ;MOVE OP1 TO Q, 2ND WORD OF
7620      C.FORK
7621
7622 203: -----
7623      J/R SVMOD           ;RESERVED MODE
7624
7625 204: -----
7626      Q,D,D,LA,           ;REGISTER. GET IT FROM LATC
7627      ID,D,SYNC,          ;SEND FIRST OP OUT FOR ACCEL
7628      C.FORK
7629
7630 224: -----
7631 B.WR: R(PRN),D,DT/INST,DEP, ;WRITE TO REGISTER
7632      SET(CC INST),        ;STORE RESULT IN REGISTER
7633      CLR,IB,OPC,           ;SET CC FROM IT
7634      PC,PC+1,J,IRD        ;AND GO DO NEXT INSTRUCTION
7635
7636 205: -----
7637      J/R SVMOD
  
```

E 1

ZZ-ESOAA-124.0 : FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame E1 Sequence 210  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 209  
 : FORKS .MIC [600,1204] I-stream decode forks : B-FORK for VAX Instructions

:7638 ;B FORK SPECIFIER EVALUATION: QUAD REGISTERS

:7639

:7640 206: :-----;

:7641 R[C1] LA, :QUAD REGISTER

:7642 ID D.SYNC, :SEND FIRST OP OUT FOR ACCEL

:7643 Q\_D :GET LOW-ADDR WORD TO T1

:7644

:7645 :-----;

:7646 D\_R(PRN+1), :GET SECOND PART

:7647 C.FORK

:7648

:7649 226: :-----;

:7650 Q\_RC[T0] :QUAD WRITE TO REGISTER

:7651 :-----; :GET LOW ADDRESS PART

:7652

:7653 R(PRN) Q, :-----;

:7654 SET.CC(INST) :STORE LOW ADDRESS PART

:7655 :-----; :SETTING TENTATIVE CONDITION CODE

:7656

:7657 R(PRN+1) D, :-----;

:7658 N AMX.Z TST, :HIGH ADDRESS PART IS IN D

:7659 C[R.IB.DPC, :GET FINAL CC, Z IS 1 IFF BOTH ZERO

:7660 PC\_PC+1,J/IRD :FORGET THIS INSTRUCTION

:7661 :-----; :MOVE ON TO NEXT

:7662 207: :-----;

:7663 J/RSMOD

:7664

:7665 208: :-----;

:7666 B.DR: Q&VA\_LA, :-----;

:7667 ID D.SYNC, :-----;

:7668 DATA.TYPE?,J/B.M :(R)

:7669

:7670 209: :-----;

:7671 R(PRN)\_LA+K[SP1.CON].RLOG, :UPDATE THE STACK POINTER

:7672 J/B.DR :THEN LOAD UN-INCREMENTED ADDR

:7673

:7674 20A: :-----;

:7675 R(PRN)\_LA-K[SP1.CON].RLOG, :-----;

:7676 Q&VA\_A[U, :-(R) AUTO DECREMENT

:7677 ID D.SYNC, :USE DECREMENTED ADDR

:7678 DATA.TYPE?,J/B.M :SEND FIRST OP OUT FOR ACCEL

:7679

:7680 20B: :-----;

:7681 Q\_D.VA\_LA, :-----;

:7682 ID\_D.SYNC :@R)+ AUTO INCREMENT DEFERED

:7683

:7684 :\*\*\*\*\*

:7685 : \* Patch no. 052, PCS 020B trapped to WCS 117A \*

:7686 :\*\*\*\*\*

:7687

:7688 :-----;

:7689 D[LONG] CACHE, :GET INDIRECT WORD

:7690 R(PRN)\_A+K[.4].RLOG, :WHILE UPDATING REGISTER

:7691 J/B.DF :THEN JOIN COMMON CODE

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204]  
; P1W124.MCR 600,1204]  
; FORKS .MIC [600,1204]

I-stream decode for 14-Jan-82  
MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124

I-stream decode forks : B-FORK for VAX Instructions

F 1

Fiche 2 Frame F1

Sequence 211

Page 210

U 020C, 0060,C07D,1580,BDB8,0000,047E

:7692 ;B FORK SPECIFIER EVALUATION: INDEX AND DISPLACEMENT MODES

:7693

:7694 20C:

:7695 RCT7] LA.CTX, :INDEX MODE, CONTEXT SHIFT INDEX  
:7696 ID.D SYNC, :SEND FIRST OP OUT FOR ACCEL  
:7697 CALL.J/ASPC ; AND GO EVALUATE BASE OPERAND ADDRESS

U 026C, 0C11,0814,01C0,F800,0200,00D0

:7698  
:7699 26C:  
:7700 Q&VA\_D+LC, :RETURN HERE FROM ASPC  
:7701 D.Q, :COMPUTE INDEXED ADDRESS  
:7702 DATA.TYPE?,J/B.M ;RESTORE FIRST OPERAND TO D  
:7703 ;GO GET THE OPERAND

U 020D, D005,2854,15C0,BC00,0200,00D0

:7704 20D:  
:7705 Q&VA\_Q+LB.PC, :D(R) DISPLACEMENT MODE.  
:7706 CLR.IB.SPEC, :DISCARD THE SPECIFIER  
:7707 ID.D SYNC, :SEND FIRST OP OUT FOR ACCEL  
:7708 DATA.TYPE?,J/B.M ;GO GET THE OPERAND

U 020F, D005,2054,15E0,BC00,0200,0118

:7709  
:7710 20F:  
:7711 Q.D,VA.Q+LB.PC, :AD(R) DISPLACEMENT DEFERRED  
:7712 ID.D SYNC, :SEND FIRST OP OUT FOR ACCEL  
:7713 CLR.IB.SPEC ;DROP THE SPECIFIER

:7714

:7715

:7716 ; \*\*\*\*\*  
:7717 ; \* Patch no. 053, PCS 020F trapped to WCS 117B \*  
:7718 ; \*\*\*\*\*

U 0118, 0000,003C,0180,4000,0000,0128

:7719  
:7720 D[LONG]\_CACHE ;GET INDIRECT, GO USE IT AS ADDR  
:7721

:7722

:7723 B.DF:

:7724 Q&VA\_D, :USE POINTER AS ADDRESS  
:7725 D.Q, ;RESTORE FIRST OPERAND TO D  
:7726 DATA.TYPE?,J/B.M ;

U , 28, 0C01,083C,01C0,F800,0200,00D0

;7726 ;HERE ARE VARIANTS OF THE B-FORK ENTRY POINTS FOR R=PC  
 ;7727  
 ;7728 214: -----;  
 ;7729 J/R SVMOD ;PC REGISTER MODE  
 ;7730  
 ;7731 215: -----;  
 ;7732 J/R SVMOD ;ILLEGAL REGISTER MODE. R=PC  
 ;7733  
 ;7734 216: -----;  
 ;7735 J/R SVMOD ;PC QUAD REGISTER MODE  
 ;7736  
 ;7737 217: -----;  
 ;7738 J/R SVMOD ;ILLEGAL QUAD REGISTER MODE, R=PC  
 ;7739  
 ;7740 218: -----;  
 ;7741 J/R SVMOD ;(PC)  
 ;7742  
 ;7743 219: -----;  
 ;7744 Q,D,D,Q, ;(PC)+ IMMEDIATE MODE  
 ;7745 ID,D,SYNC, ;SEND FIRST OP OUT FOR ACCEL  
 ;7746 CLR,IB,SPEC,  
 ;7747 DATA,TYPE?,J/B,I ; BEWARE ADDRESS SOURCES  
 ;7748  
 ;7749 21A: -----;  
 ;7750 J/R SVMOD ;-(PC)  
 ;7751  
 ;7752 21B: -----;  
 ;7753 VA\_Q, ;@ (PC)+ ABSOLUTE MODE  
 ;7754 ID,D,SYNC, ;SEND FIRST OP OUT FOR ACCEL  
 ;7755 CLR,IB,SPEC,  
 ;7756 DATA,TYPE?,J/B,M  
 ;7757  
 ;7758 21C: -----;  
 ;7759 J/R SVMOD ;INDEX MODE, R=PC  
 ;7760  
 ;7761 21D: -----;  
 ;7762 J/R SVMOD ;NESTED INDEX MODE, R=PC  
 ;7763  
 ;7764 21E: -----;  
 ;7765 RC[T1] Q, ;QUAD IMMEDIATE  
 ;7766 Q\_IB,DATA, ;GET SECOND PART  
 ;7767 C[R,IB,COND, ;DISCARD IT FROM IB  
 ;7768 PC,PC+4, ;STEP PC OVER SECOND PART OF LITERAL  
 ;7769 IB,TEST?,J/B,IQ ;MAKE SURE IT'S ALL THERE

ZZ-ESOAA-124.0 : FORKS .MIC [600,1204] H 1  
: P1W124.MCR 600,1204] MICRO2 1L(03) I-stream decode for 14-Jan-82 Fiche 2 Frame H1 Sequence 213  
: FORKS .MIC [600,1204] I-stream decode forks : B-FORK for VAX Instructions VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 212

U 0287, 0000.003D.0180,F800,0000.0EE0 :7770 :HERE OFF B-FORK WHEN INSTRUCTION DECODE ROMS INDICATE SHOULD NOT DO BFORK  
:7771  
:7772 287: :-----; SHOULD NEVER HAPPEN  
:7773 CALL,J/EH.US EQ ;GET A MACHINE CHECK  
:7774  
:7775 :\*\*\*\*\*  
:7776 : \* Patch no. 073, PCS 0287 trapped to WCS 1181 \*  
:7777 :\*\*\*\*\*  
:7778  
:7779 :HERE OFF B-FORK, WHEN INSTRUCTION BUFFER DOES NOT HAVE ENOUGH DATA  
U 027C, 0000.003D.0180,F800,0000.0E64 :7780  
:7781 27C: :-----;  
:7782 CALL,J/IB.TBM ;TB MISS. REFILL IT  
:7783  
U 027D, 0000.003D.0180,F800,0000.0B80 :7784  
:7785 27D: :-----;  
:7786 CALL,J/IB.ERR ;ANY ERROR. FIND OUT WHAT HAPPENED  
:7787 27E: :-----;  
U 027E, F000.003F.01F0,F847,0000.0200 :7788 MCT/ALLOW.IB.READ,  
:7789 B.FORK ;STALL. WAIT FOR THE DATA TO COME IN

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Sequence 214  
 : FORKS .MIC [600,1204] I-stream decode forks : B-FORK for VAX Instructions Page 213

:7790 ;HERE FOR THE SECOND AND SUBSEQUENT STATES OFF B-FORK  
 :7791  
 :7792  
 :7793 =000 ;-----;GET HERE BY DATA.TYPE?  
 :7794 B.M: ALU D.SET.CC(INST).;WRITE DESTINATION  
 :7795 CACHE D.INST.DEP.;SET CONDITION CODES ON RESULT  
 :7796 CLR.IB.OPC.;STORE RESULT  
 :7797 PC\_PC+1,J/IRD.;GO DO NEXT INSTRUCTION  
 :  
 :7798  
 :7799  
 :7800 Q\_D.;STORE QUAD/DOUBLE RESULT  
 :7801 D\_RC[T0].;GET LOW ADDRESS PART TO STORE FIRST  
 :7802 J7B.WQ.;THEN STORE HIGH ADDRESS PART  
 :  
 :7803  
 :7804 =100 ;-----;READ OR MODIFY  
 :7805 RC[T7]\_Q.;SAVE OPERAND ADDRESS  
 :7806 Q\_D.;SAVE FIRST OPERAND IN Q  
 :7807 D\_CACHE.INST.DEP.;GET NORMAL B, W, L, OR F DATA  
 :7808 C.FORK.;GO EXECUTE  
 :  
 :7809  
 :7810 RC[T7]\_Q.;QUAD/DOUBLE  
 :7811 Q\_D.;OPERAND ADDRESS TO T7  
 :7812 D\_CACHE.INST.DEP.;FIRST OP TO Q, MAKE ROOM FOR SECOND  
 :7813 J7B.MQ.;GET FIRST LONGWORD OF QUAD/DOUBLE  
 :  
 :7814  
 :7815  
 :7816 Q\_D,D\_Q.;-----;FIELD SOURCE  
 :7817 C.FORK.;FIRST OP TO Q, ADDR OF SECOND TO D  
 :  
 :7818  
 :7819  
 :7820 Q\_D,D\_Q.;-----;ADDRESS SOURCE  
 :7821 C.FORK.;FIRST OP TO Q, ADDRESS TO D  
 :  
 :7822  
 :7823  
 :7824 =:END OF DATA.TYPE BRANCH

ZZ-ES0AA-124.0 ; FORKS .MIC [600,1204]  
: P1W124.MCR 600,1204]  
: FORKS .MIC [600,1204]

J 1  
I-stream decode for 14-Jan-82  
MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124

Fiche 2 Frame J1

Sequence 215

Page 214

I-stream decode forks : B-FORK for VAX Instructions

U 012B, 0001.007C,1580,BD88,0000,013D

:7825 ;HERE TO READ SECOND LONGWORD OF A QUAD/DOUBLE OPERAND  
:7826  
:7827  
:7828 B.MQ: RC[T1] D, :STORE FIRST PART OF QUAD/DOUBLE OP  
:7829 ID\_D\_SYNC, :SEND IT TO ACCELERATOR  
:7830 VA\_VA+4 :GET ADDRESS OF SECOND PART  
:7831  
:7832  
:7833 D[LONG]\_CACHE, :GET SECOND PART OF QUAD/DOUBLE  
:7834 C.FORK :GO EXECUTE WITH IT  
:7835  
:7836 ;HERE TO STORE QUAD/DOUBLE RESULT INTO MEMORY, SETTING CONDITION CODES  
:7837  
:7838  
:7839 B.WQ: CACHE\_D.INST.DEP, :STORE QUAD/DOUBLE RESULT  
:7840 ALU\_D,SET.CC(INST) :SETUP TENTATIVE CC FROM RESULT  
:7841  
:7842  
:7843 D\_Q, :GET HIGH-ADDRESS DATA  
:7844 VA\_VA+4 :AND GO WRITE IT  
:7845  
:7846  
:7847 CACHE\_D[LONG], :STORE SECOND PART OF QUAD RESULT  
:7848 ALU\_D,N AMX.Z\_TST. :Z=1 IFF BOTH PARTS ZERO  
:7849 CLR\_IB.Opcode :GO BACK TO IRD  
:7850 PC\_PC+1,J/IRD

U 013D, 0000.003F,0180,4070,0000,0300

U 0154, 0001.003C,0180,30C0,0070,0161

U 0161, 0C00.003C,0180,F803,0000,0164

U 0164, C001.003C,0180,3004,4030,0062

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] K 1  
 : P1W124.MCR 600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame K1  
 : FORKS .MIC [600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Sequence 216  
 Page 215

I-stream decode forks : B-FORK for VAX Instructions

	:7851	;HERE FOR QUAD/DOUBLE I-STREAM LITERALS
	:7852	;THE FIRST LONGWORD OF LITERAL IS IN T1 ALREADY, WE'VE TRIED TO READ THE
	:7853	;SECOND LONGWORD, AND HERE WE TEST TO SEE IF WE GOT IT.
	:7854	
	:7855	=00 -----;
U 01E0, 0000,003D,0180,F800,0000,0E64	:7856	B.IQ: CALL,J/IB.TBM ;ISTREAM HAD A TB MISS
	:7857	
U 01E1, 0000,003D,0180,F800,0000,0B80	:7858	-----;I BUFFER STOPPED FOR AN ERROR
	:7859	
	:7860	
U 01E2, F000,0B3C,01F0,F800,0000,01E0	:7861	-----;
	:7862	Q IB.DATA.CLR.IB2-5, ;STALL WAITING FOR THE DATA
	:7863	IB.TEST?,J/B.IQ ;LOOP UNTIL IT ARRIVES
	:7864	
	:7865	-----;
U 01E3, DC00,087C,15E0,BC00,0000,00E5	:7866	D Q,Q,D. ;LEAVE IT IN D, MOVE FIRST OP TO Q
	:7867	ID D SYNC, ;SEND FIRST OP OUT FOR ACCEL
	:7868	CLR IB SPEC, ;GOT IT, CLEAR IT
	:7869	DATA TYPE?
	:7870	
U 00E5, 0000,003F,0180,F800,0000,0300	:7871	=101 -----;
	:7872	B.I: C.FORK ;NORMAL SRC, GO USE IT
	:7873	
U 00E7, 0814,0038,0180,F800,0000,016A	:7874	-----;
	:7875	D PC ;ADDRESS SOURCE. FIGURE OUT ADDR
	:7876	
	:7877	-----;
U 016A, 0819,003,1580,F800,0000,0300	:7878	D D~K[SP1.CON], ;BY SUBTRACTING SIZE FROM CURRENT PC
	:7879	C.FORK

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame L1 Sequence 217  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPL1.0E, WCS124 Page 216  
 : FORKS .MIC [600,1204] I-stream decode forks : B-FORK for VAX Instructions

U 02C0, 401D,E00C,0180,F8C5,4070,0062      L 1  
 :7880 ;HERE FOR CERTAIN 3-OPERAND INTEGER AND BOOLE INSTRUCTIONS  
 :7881 ; NAMELY ADDx3, SUBx3, BISx3, BICx3, XORx3 FOR x=B, W, L  
 :7882 ; WITH THE SECOND SPECIFIER SHORT LITERAL, AND THE THIRD REGISTER MODE.  
 :7883  
 :7884 2C0: ;-----  
 :7885    ALU.Q[INST.DEP]D, ;SL-R OPERATION  
 :7886    R(SP1) ALU,  
 :7887    SET.CC(INST),  
 :7888    CLR.IBO-1,  
 :7889    PC\_PC+2,J/IRD ;DROP OPCODE & DST SPEC  
 :7890  
 :7891 ;HERE FOR CERTAIN 3-OPERAND INTEGER AND BOOLE INSTRUCTIONS  
 :7892 ; NAMELY ADDx3, SUBx3, BISx3, BICx3, XORx3 FOR x=B, W, L  
 :7893 ; WITH BOTH SECOND AND THIRD SPECIFIERS INDICATING REGISTER MODE OPERANDS.  
 :7894  
 :7895 2C4: ;-----  
 :7896    ALU.LA[INST.DEP]D, ;R-R OPERATION  
 :7897    R(SP1) ALU,  
 :7898    SET.CC(INST),  
 :7899    CLR.IBO-1,  
 :7900    PC\_PC+2,J/IRD ;CC ARE INSTR DEPENDENT  
 :7901  
 :7902 ;HERE FOR CERTAIN INTEGER INSTRUCTIONS WHICH DO NOT WRITE A DESTINATION,  
 :7903 ; NAMELY BITB, BITW, BITL, CMPB, CMPW, CMPL  
 :7904 ; WITH THE SECOND SPECIFIER REGISTER MODE.  
 :7905  
 :7906 2AF: ;-----  
 :7907    BIT.R:  
 :7908    CMP.R: ALU.LA[INST.DEP]D, ;OPERATE REGISTER AGAINST MEM  
 :7909    SET.CC(INST), ;SET THE CONDITION CODES IN PSL  
 :7910    CLR.IB.OPC, ;DISCARD OP, DO NEXT INSTR  
 :7911    PC\_PC+1,J/IRD  
 :7912  
 :7913 ;HERE FOR CERTAIN INTEGER AND BOOLE INSTRUCTIONS WHICH WRITE A DESTINATION,  
 :7914 ; NAMELY ADDx2, SUBx2, BISx2, BICx2, XORx2  
 :7915 ; FOR x=B, W, L, AND ADWC, SBWC  
 :7916 ; WITH THE SECOND SPECIFIER REGISTER MODE.  
 :7917  
 :7918 227: ;-----  
 :7919    ALU.LA[INST.DEP]D, ;MEM-R OPERATION  
 :7920    R(PRN) ALU, ;RESULT INTO DST REGISTER  
 :7921    SET.CC(INST),  
 :7922    CLR.IB.OPC, ;SET CONDITION CODES ACCORDINGLY  
 :7923    PC\_PC+1,J/IRD ;GO DO NEXT INSTR

J 02AF, C01C,E00C,0180,F804,4070,0062

U 0227, C01C,E00C,0180,F8DC,4070,0062

ZZ-ES0AA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame M1 Sequence 218  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FPPKS .MIC [600,1204] I-stream decode forks : B-FORK for VAX Instructions

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	:7924	;HERE FOR AOBLS, AOBLEQ WHEN DESTINATION IS REGISTER	
	:7925		
	:7926	223: -----;	
	:7927	AOB.R: Q.D,	:SAVE LIMIT IN Q
	:7928	R7PRN)_LA+K[.1].RLOG,	:UPDATE THE DESTINATION REGISTER
	:7929	D_ALU,	:COPY IT FOR COMPARE
	:7930	SET.CC(LONG)	:SET CONDITION CODES FROM INDEX
	:7931		
	:7932		
	:7933	ALU_D-Q,	:COMPARE INDEX TO LIMIT
	:7934	CLK.UBCC,	:SAVE RESULT FOR BRANCH
	:7935	Q_IB.BDEST,	:GET BDEST FROM IB
	:7936	PC PC+1,	:STEP PC OVER IT
	:7937	IB.TEST?	:DOES IB HAVE THE DATA?
	:7938		
	:7939	=00 -----;	
	:7940	AOB.R1: CALL,J/IB.TBM	:IB STOPPED FOR TB MISS
	:7941		
	:7942		
	:7943	CALL,J/IB.ERR	
	:7944		
	:7945		
	:7946	Q_IB.BDEST,	
	:7947	IB.TEST?,J/AOB.R1	
	:7948		
	:7949		
	:7950	Q_Q+PC,	:COMPUTE BRANCH DESTINATION
	:7951	CTR.IB0-1,	:BUT ASSUME NO BRANCH
	:7952	PC PC+1,	:ADVANCE PC TO NEXT IN LINE
	:7953	ALU?,J/AOB.2	:FIND OUT WHETHER TO BRANCH

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204]  
: P1W124.MCR 600,1204]  
: FORKS .MIC [600,1204]

MICR02 1L(03) I-stream decode for14-Jan-82  
14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124

Fiche 2 Frame N1

Sequence 219

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I-stream decode forks : B-FORK for VAX Instructions

U 02A8, 7019,0824,8DF0,F80<,0010,0230

:7954 ;HERE FOR BBS, BBC, BBSS, BBCS, BBSC, BBCC, BBSSI, BBCCI  
:7955 ;WHEN BIT IS IN A REGISTER  
:7956 ;D CONTAINS THE POSITION OPERAND (A LONGWORD), AND LA CONTAINS THE  
:7957 ;REGISTER SELECTED BY THE SECOND SPECIFIER.

U 0230, 9000,003D,0180,F800,0000,0E64

:7959 2A8: -----  
:7960 BB.R: ALU.D.ANDNOT.K[.1F], ;TEST POSITION FOR LESS THAN 32  
:7961 CLK.UBCC, ;SETTING ALU Z IF SO  
:7962 C\_IB.BDEST, ;GET BDEST TO Q  
:7963 PC PC+1, ;STEP PC PAST IT  
:7964 IB.TEST? ;CHECK THAT WE GOT BDEST

U 0231, 0000,003D,0180,F800,0000,0880

:7965 -----  
:7966 =0 BB.R1: CALL,J/IB.TBM  
:7967 -----  
:7968 -----  
:7969 -----  
:7970 CALL,J/IB.ERR  
:7971 -----  
:7972 -----  
:7973 Q\_IB.BDEST,  
:7974 IB.TEST?,J/BB.R1  
:7975 -----  
:7976 CLR.IB.SPEC, ;DISCARD BDEST FROM IB BYTE 1  
:7977 SC\_D. ;GET BIT POSITION INTO SC  
:7978 Z? ;CHECK THAT IT IS LESS THAN 32

U 0233, D001,013C,0180,F800,0082,0020

:7979 -----  
:7980 -----  
:7981 =0 FN.ABS.20:  
:7982 -----  
:7983 J/I:SVOPR ;ALU Z=0  
:7984 ----- ;POSITION .GEQ. 32, RESERVED OPERAND

U 0020, 00C:,003C,0180,F800,0000,0106

:7985 -----  
:7986 ----- ;ALU Z=1 (POSITION .LSS. 32)  
:7987 ALU\_LA.ANDNOT.MASK, ;TEST SELECTED BIT OF REGISTER  
:7988 CLK.UBCC ;SET Z ACCORDINGLY

U 0021, 0070,0024,0180,F800,0010,0191

:7989 -----  
:7990 R'PRN)\_LA[INST.DEP]MASK, ;MODIFY THE BIT AS REQUIRED  
:7991 ALU? ;TEST WHETHER TO BRANCH

U 0191, 0000,1B0C,0180,F8D8,0000,00E9

:7992 -----  
:7993 =1001 -----  
:7994 PC&VA\_Q+PC,FLUSH.IB,J/IB.FILL ;Z=0, BBS

U 00E7, 2015,2014,0180,F801,4200,00AB

:7995 -----  
:7996 -----  
:7997 CLR.IB.OPC, ;Z=0, BBC  
:7998 PC\_PC+1,J/IRD

U 00EB, C000,0C3C,0180,F804,4000,0062

:8000 -----  
:8001 CLR.IB.OPC, ;Z=1, BBS  
:8002 PC\_PC+1,J/IRD

U 00ED, C000,003C,0180,F804,4000,0062

:8003 -----  
:8004 CLR.IB.OPC, ;Z=1, BBS  
:8005 PC\_PC+1,J/IRD

U 00FF, 2015,2014,0180,F801,4200,00AB

:8006 -----  
:8007 PC&VA\_Q+PC,FLUSH.IB,J/IB.FILL ;Z=1, BBC

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] !-stream decode for 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FORKS .MIC [600,1204] I-stream decode forks : B-FORK for VAX Instructions

B 2

Fiche 2 Frame B2

Sequence 220

Page 219

U 024D, C001,C03C,0180,F804,4070,0062

```
:8007 ;B-FORK EXECUTIONS
:8008
:8009 ;HERE FOR TSTB, TSTW, TSTL
:8010 ; THE SOURCE OPERAND IS IN D.
:8011
:8012 24D: ;-----;
:8013 TST: ALU_D,SET.CC(INST). ;JUST SET CC FROM DATA
:8014 CLR,IB,OPC
:8015 PC,PC+1,J,IRD
:8016
:8017 ;HERE FOR INCx, DECx, FOR x= B, W, L AND DESTINATION NOT REGISTER
:8018 ; THE DESTINATION OPERAND IS IN D
:8019
:8020 24E: ;-----;
:8021 INC:
:8022 DEC: D,D[INST.DEP]Q. ;OPERATE ON DATA IN D
:8023 SET.CC(INST). ;SET CC IN PSL ACCORDINGLY
:8024 J/STORE ;STORE IT ACCORDING TO VA
:8025
:8026 ;HERE FOR PUSHL AND PUSHAB, PUSHAW, PUSHAL, PUSHAD
:8027 ; D CONTAINS THE SOURCE OPERAND (ADDRESS, IN THE CASE OF PUSHAD)
:8028
:8029 248: ;-----;
:8030 PUSHL:
:8031 PUSHAD: ALU_D,SET.CC(INST). ;SET PSL CC FROM DATA TO TOP
:8032 LAB_R[SP] ;GET SP READY TO DECREMENT
:8033
:8034
:8035 R[SP]&VA_LA-K[E].RLOG, ;LOAD DECREMENTED SP INTO VA
:8036 J/STORE
:8037 ;HERE FOR JSB. JUMP ADDRESS IS IN D
:8038
:8039
:8040 28F: ;-----;
:8041 JSB: Q,D, ;JUMP ADDR TO Q,
:8042 D,PC, ;GET PC TO SAVE
:8043 LAB_R[SP] ;GET STACK POINTER INTO LATCH
:8044
:8045
:8046 R[SP]&VA_LA-K[E].RLOG ;DECREMENT SP INTO VA
:8047
:8048
:8049 CACHE,D[LONG], ;STORE PC ON THE STACK
:8050 J/JMP,Q ;AND JUMP TO ADDR IN Q
:8051
:8052 ;HERE ON JMP. JUMP ADDRESS IS IN D
:8053
:8054 28E: ;-----;
:8055 JMP: PC&VA_D, ;LOAD NEW ADDRESS
:8056 FLUSH,IB,
:8057 J/IB,ILL
```

U 028F, 0814,0038,01E0,FA70,0000,01A4

U 01A4, 0018,0004,1180,FAF0,0200,01BC

U 01BC, 0000,003C,0180,3000,0000,0163

U 028E, 2001,003C,0180,F801,4200,00AB

ZZ-ES0AA-124.0 : FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame C2 Sequence 221  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FORKS .MIC [600,1204] I-stream decode forks : B-FORK for VAX Instructions

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	:8058	;HERE FOR BLBS, BLBC	
	:8059	; THE SOURCE OPERAND IS IN D	
	:8060		
	:8061	2CF: -----	
	:8062	BLB: ALU_D[INST.DEP]K[.1],	:TEST LOW BIT FOR SET OR CLR
	:8063	CLK_UBCC,	:SET ALU Z BIT ACCORDINGLY
	:8064	Q_IB.BDEST,	:GET BRANCH DISP
	:8065	PC_PC+1,	
	:8066	IB.TEST?	:SEE IF WE GOT IT
	:8067		
U 02CF, 7019,080C,05F0,F804,0010,0388	:8068	=00 :00-----	:TB MISS
	:8069	BLB.1: CALL,J/IB.TBM	:GO FILL IN TB, IT DOESN'T KNOW
	:8070		
U 0388, 0000,003D,0180,F800,0000,0E64	:8071	:01-----	:IB ERROR
	:8072	CALL,J/IB.ERR	:IBUFFER STOPPED FOR AN ERROR
	:8073		
U 0389, 0000,003D,0180,F800,0000,0B80	:8074	:10-----	:STALL
	:8075	Q_IB.BDEST,	:WAIT FOR DATA
	:8076	IB.TEST?.J/BLB.1	:TEST FOR ARRIVAL OF BDEST
	:8077		
	:8078		
	:8079	D_Q+PC,	:COMPUTE BRANCH ADDR
	:8080	CIR.IB0-1,	:DISCARD OPCODE IN CASE NO BRANCH
U 038B, 4815,2114,0180,F804,4000,00A0	:8081	PC_PC+1,	:AND STEP PC TO NEXT
	:8082	Z?	:SHOULD WE BRANCH?
	:8083		
	:8084	=0 -----	:Z=0
U 00A0, 2001,003C,0180,F801,4200,00AB	:8085	PC&VA_D,	:TAKE THE BRANCH
	:8086	FLUSH.IB,J/IB.FILL	
	:8087		
U 00A1, F80C,003B,01F1,F857,139B,6000	:8088		:Z=1
	:8089	IRD	:DON'T BRANCH

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame D2 Sequence 222  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 221  
 : FORKS .MIC [600,1204] I-stream decode forks : B-FORK for VAX Instructions

D 2

```

:8090 ;HERE FOR SOBGTR, SOBGEQ WHEN DESTINATION IS NOT REGISTER
:8091 ; THE DESTINATION OPERAND IS IN D
:8092
:8093 =0CE: ;-----;
:8094 SOB: D,D-K[.1], :DECREMENT THE OPERAND
:8095 SET.CC(LONG), :GET BRANCH CONDITION
:8096 Q,IB.BDEST, :GET & CLR BRANCH DISPLACEMENT FROM IB
:8097 PC,PC+1,
:8098 IB.TEST? ;SEE IF WE GOT IT OK
:8099
:8100 =00 ;-----;
:8101 SOB.1: CALL,J/IB.TBR
:8102
:8103 ;-----;
:8104 CALL,J/IB.ERR
:8105
:8106 ;-----;
:8107 Q,IB.BDEST, :WAIT FOR IBUFFER TO GET BDEST
:8108 IB.TEST?,J/SOB.1 ;LOOP TESTING
:8109
:8110 ;-----;
:8111 [CACHE D[LONG]], :STORE RESULT IN MEMORY
:8112 CLR,IB.SPEC, :DISCARD BDEST FROM IB BYTE 1
:8113 Q,Q+PC, :COMPUTE BRANCH ADDRESS
:8114 PSL.CC? ;BRANCH?
:8115
:8116 =0011 ;-----;N=0, Z=0
:8117 JMP.Q: ;-----;ALSO USED BY JSB
:8118 SOB.2: PC&VA_Q,FLUSH,IB,J/IB.FILL ;RESULT GTR, SO BRANCH
:8119
:8120 ;-----;N=0, Z=1
:8121 CLR,IB,OPC,PC,PC+1,
:8122 IR0?,J/SOB.3 ;BRANCH IFF SOBGEQ
:8123
:8124 ;-----;N=1, Z=0
:8125 CLR,IB,OPC,PC,PC+1,
:8126 /IRD ;RESULT LSS, DO NOT BRANCH
:8127
:8128 =;END PSL.CC TEST
:8129
:8130 =1101 ;-----;IR0=0
:8131 SOB.3: PC&VA_Q,FLUSH,IB,J/IB.FILL ;SOBGEQ BRANCHES ON ZERO
:8132
:8133 ;-----;IR0=1
:8134 IRD ;SOBGTR DOES NOT BRANCH ON ZERO

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ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204]  
; P1W124.MCR 600,1204]  
; FORKS .MIC [600,1204]

I-stream decode for 14-Jan-82  
MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124

Fiche 2 Frame E2

Sequence 223

Page 222

U 028B, 0803,403C,3DF0,2C00,0000,01D5

:8135 ;HERE FOR BISPSW AND BICPSW  
:8136 ; THE SOURCE OPERAND IS IN D  
:8137  
:8138 28B: -----;  
:8139 BISPSW:  
:8140 BICPSW: Q\_1D[PSL], ;GET PSL READY FOR MODIFICATION  
:8141 D\_D.OXT[WORD] ;DISCARD GARBAGE FROM WORD OPERAND

U 01D5, 081D,380C,0180,F800,0000,0289

:8142  
:8143 -----;  
:8144 D\_4[INST.DEP]D, ;SETUP F^L  
:8145 D.B1? ;IS BYTE 1 CLEAR?

U 02B9, C000,003C,3D80,3C04,4000,0062

:8146 =01 :0-----;BYTE 1.EQL.0  
:8147 ID[PSL] D, ;WRITE BACK PSL  
:8148 CLR.IB.0PC  
:8149 PC\_PC+1,J/IRD

U 02BB, 0000,003C,0180,F800,0000,0106

:8150  
:8151 :1-----;BYTE 1.NEQ.0  
:8152 J/RSPVOPR ;TAKE RESERVED OPERAND TRAP

:8153  
:8154 :HERE FOR MNEGx, MCOMx FOR x=B, W, L  
:8155 ; THE SOURCE OPERAND IS IN D

U 0249, F81D,E00F,01F0,F847,0070,0300

:8156  
:8157 249: -----;  
:8158 MNEG:  
:8159 MCOM: D\_Q[INST.DEP]D, ;OPERATE ON D  
:8160 SET.CC(INST), ;LOAD PSL CC ON FUNCTION  
:8161 WRITE.DEST,J/WRD ;GO EVALUATE DEST SPECIFIER

U 024A, F803,C03F,01F0,F847,00C0,0200

:8162  
:8163 :HERE FOR MOVZBW, MOVZBL, MOVZWL  
:8164 ; THE SOURCE OPERAND IS IN D  
:8165  
:8166 24A: -----;  
:8167 MOVZ: D\_D.OXT[INST.DEP], ;ZERO EXTEND THE SOURCE OPERAND TO LONG  
:8168 B.FORK ;GO WRITE THAT RESULT AS MOVE WOULD

:8169

ZZ-ESOAA-124.0 ; FORKS .MIC [600.1204] I-stream decode for 14-Jan-82 F 2  
 : P1W124.MCR 600.1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Sequence 224  
 : FORKS .MIC [600.1204] I-stream decode forks : B-FORK for VAX Instructions Page 223

	:8170	;HERE FOR ADAWI	
	:8171	;ADD ALIGNED WORD INTERLOCKED	
	:8172	; D CONTAINS SOURCE	
	:8173		
	:8174	20E: -----	
U 020E, 0000.003D,1980,F800,0084,647E	:8175	ADAWI: SC K[ZERO]	;CLEAR SC FOR BRANCH ON RETURN
	:8176	CALL,J/ASPC	;EVALUATE DESTINATION ADDRESS
	:8177		
U 026E, 0000.0C3C,0180,F800,0000,00D2	:8178	26E: -----	;RETURN HERE WITH MEMORY OPERAND
	:8179	MUL?,J/ADA.1	;TEST ALIGNMENT OF DESTINATION
	:8180		
U 026F, C01C,C014,0180,F8DC,4070,0062	:8181	26F: -----	;RETURN HERE WITH REGISTER OPERAND
	:8182	R(PRN) LA+Q,	;PUT RESULT IN REGISTER
	:8183	SET.CC(INST),	
	:8184	PC PC+1,CLR.IB.OPC,	;MOVE ON TO NEXT INSTRUCTION
	:8185	J/IRD	
	:8186		
U 00D2, 0000.403C,0180,7000,0000,01F3	:8187	=10 ADA.1: -----	;DO=0, DEST IS WORD ALIGNED
	:8188	D[WORD]_CACHE.LK,	;GET DEST INTERLOCKED
	:8189	J/ADA.2	
	:8190		
U 00D3, 0000.003C,0180,F800,0000,0106	:8191	-----	;DO=1, UNALIGNED
	:8192	J/RSVOPR	
	:8193		
U 01F3, 081D,C014,0180,F800,0070,01F9	:8194	-----	
	:8195	ADA.2: D_D+Q,SET.CC(INST)	;ADD SOURCE TO DESTINATION
	:8196		
	:8197	-----	
U 01F9, C000.403C,0180,3804,4000,0062	:8198	CACHE_D[WORD].LK,	;WRITE IT BACK
	:8199	CLR.IB.OPC,PC_PC+1,J/IRD	;GO TO NEXT INSTRUCTION

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame G2 Sequence 225  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 224  
 ; FORKS .MIC [600,1204] I-stream decode forks : B-FORK for VAX Instructions

G 2

U 028C, C010,C038,0180,F904,4870,0062	:8200 ;FLOAT/DDOUBLE EXECUTIONS WITH SINGLE OPERAND	
	:8201	
	:8202 28C: -----;TSTD	
	:8203 TSTD: ALU_RC[T0].SET.CC(INST), ;SET CONDITION CODES FROM SOURCE	
	:8204 CHK.FLT.OPR, ;FAULT IF RESERVED OPERAND	
	:8205 CLR.IB.OPC,PC_PC+1,J/IRD ;GO TO NEXT INSTRUCTION	
	:8206	
	:8207 28D: -----;TSTF	
	:8208 TSTF: ALU_D.SET.CC(INST), ;SET CONDITION CODES FROM SOURCE	
	:8209 CHK.FLT.OPR, ;FAULT IF RESERVED OPERAND	
	:8210 CLR.IB.OPC,PC_PC+1,J/IRD ;GO TO NEXT INSTRUCTION	
	:8211	
	:8212 285: -----;MOVF, MNEGFI	
	:8213 MOVF: ;	
	:8214 MNEGFI: SC_D(EXP), ;GET EXPONENT FOR ZERO TEST	
	:8215 CHR.FLT.OPR, ;CATCH RESERVED OPERANDS	
	:8216 D.BYTES?,J/MOVD.2 ;IS EXPONENT ZERO (CRUDELY)?	
	:8217	
	:8218 241: -----;	
	:8219 MOVD: ;	
	:8220 MNEGDI: Q_D, ;SAVE LOW-ORDER FRACTION BITS	
	:8221 D_RC[T0], ;GET OUT HIGH PART WITH EXPONENT	
	:8222 CHK.FLT.OPR, ;ABORT IF RESERVED OPERAND	
	:8223 SC_ALU(EXP),J/MOVD.3 ;CATCH EXPONENT FOR ZERO TEST	
	:8224	
	:8225 =1000 ;SET UP CONSTRAINT BLOCK	
	:8226 =1011 ;SC_EQL. 0 ON 'MUL?' TEST AT MOVD.3	
	:8227 MOVD.1: Q_0,RC[T1] K[ZERO], ;CLEAN UP POTENTIALLY DIRTY ZERO	
	:8228 SET.CC(INST),J/WRQ.DST	
	:8229	
	:8230 =1100 ;D<15:0>.EQL. 0	
	:8231 MOVD.2: D_0,ALU_K[ZERO], ;RESULT IS FLOATING ZERO	
	:8232 SET.CC(INST), ;SET CONDITION CODES TO ZERO	
	:8233 WRITE.DEST,J/WRD	
	:8234	
	:8235 =1101 ;D BYTE 1 .EQL. 0 (IF MOVF, MNEGFI)	
	:8236 MOVD.3: RC[T1] Q, ;SAVE LOW-ORDER WHERE CFORK CAN FIND	
	:8237 MUL?,J7MOVD.1 ;IS THE EXPONENT (IN SC) ZERO?	
	:8238	
	:8239 =1110 ;D BYTE 1 .NEQ. 0 IN MOVF, MNEGFI	
	:8240 D_D[INST.DEP]K[.8000], ;TRANSFORM SIGN IF MNEG	
	:8241 SET.CC(INST), ;SET CONDITION CODES FROM DEST	
	:8242 WRITE.DEST,J/WRD ;STORE THAT	
	:8243	
	:8244 =1111 ;SC_NEQ. 0 OR D BYTES 180 .NEQ. 0	
	:8245 D_D[INST.DEP]K[.8000], ;TRANSFORM SIGN IF MNEG	
	:8246 SET.CC(INST), ;SET CONDITION CODES FROM DEST	
	:8247 WRITE.DEST,J/WRD ;STORE THAT	

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82  
; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS  
; FORKS .MIC [600,1204] I-stream decode forks : B-FORK for VAX Instructions

H 2

Fiche 2 Frame H2

Sequence 226

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U 024C, F802,C03F,01F0,F847,0000,0200      :8248 ;HERE FOR CVTBW, CVTBL, CVTLW, WITH THE SOURCE OPERAND IN D  
; THEY ARE EASY, BECAUSE "THE" NEED ONLY SIGN EXTEND THE SOURCE  
:8249  
:8250  
:8251 24C: -----;  
:8252 CVTBW:  
:8253 CVTBL:  
:8254 CVTLW: D\_D.SXT[INST.DEP].      :SIGN EXTEND THE SOURCE TO LONG  
:8255 B.FORK      ;GO WRITE THAT AS MOVE WOULD  
:8256  
:8257 ;HERE FOR CVTWB, CVTLB, CVTLW, WITH THE SOURCE OPERAND IN D  
; THEY'RE TOUGHER, BECAUSE WE MUST CHECK FOR OVERFLOW  
:8258  
:8259  
:8260 24B: -----;  
:8261 CVTLW:  
:8262 CVTLB:  
:8263 CVTWB: Q\_D.SXT[INST.DEP].      :MAKE BYTE LONG  
:8264 NZ ALU.V&C.0.      ;SET CC ON IT (DEST RESULT)  
:8265 SUB7SPEC.J/CVT.2      ;ADVANCE EXEC PT CTR FOR NEW CONTEXT  
:8266  
:8267  
:8268 U 024B, 0002,C03F,01C0,F800,0050,0286      CVT.2: -----;  
:8269      ALU\_D.XOR.Q.SET.(CC(INST)).      ;SET V IF SOURCE DATA TYPE (IN D)  
:8270      WRITE.DEST.J/WRD      ;NOT EQL TO DST DATA TYPE IN Q  
; GO STORE RESULT  
U 0286, F01D,C023,01F0,F847,0070,0300

I 2

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame I2 Sequence 227  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 226  
 ; FORKS .MIC [600,1204] I-stream decode forks : C-FORK for VAX Instructions

:8271 .TOC " I-stream decode forks : C-FORK for VAX Instructions"  
 :8272  
 :8273 :Control passes here from any 'C.FORK' state.  
 :8274 :The state of the data path is:  
 :8275 :      LA & LB = Register selected by second specifier  
 :8276 :      VA    = address of second operand  
 :8277 :      D      = second operand  
 :8278 :      Q      = first operand  
 :8279  
 :8280 :Unlike A and B forks, specifier evaluation here is by subroutine call.  
 :8281 : Instructions with two or more operands go to execution at  
 :8282 : C fork. Those which have three or more call either the SPEC or ASPC  
 :8283 : subroutines to evaluate specifiers after the first two.  
 :8284  
 :8285  
 :8286 :HERE FOR 2-OPERAND INTEGER INSTRUCTIONS WHICH DO NOT WRITE A DESTINATION,  
 :8287 :NAMELY BITB, BITW, BITL, CMPB, CMPW, CMPL  
 :8288 :WHEN THE SECOND SPECIFIER IS MEMORY OR SHORT LITERAL  
 :8289  
 :8290 349: :-----:  
 :8291 :BIT:  
 :8292 :CMP:    ALU\_D[INST.DEP]Q, :OPERATE ON OPERANDS  
 :8293 :       SET.CC(INST), :CONDITION CODES ARE ONLY RESULT  
 :8294 :       CLR.IB.OPC, :DISCARD OP, DO NEXT INSTRUCTION  
 :8295 :       PC\_PC+1,J/IRD  
 :8296  
 :8297 :HERE FOR 2-OPERAND INTEGER AND BOOLE INSTRUCTIONS WHICH WRITE A DESTINATION,  
 :8298 :NAMELY ADDx2, SUBx2, BISx2, BICx2, XORx2, MNNEGx, MOVx, MCOMx  
 :8299 :FOR x = B, W, L, PLUS ADWC, SBWC  
 :8300 :WHEN THE SECOND SPECIFIER IS MEMORY  
 :8301  
 :8302 348: :-----:  
 :8303 :D\_D[INST.DEP]Q, :DO THE OPERATION  
 :8304 :SET.CC(INST), :SET PSL<NZVC> ACCORDINGLY  
 :8305 :J/STORE  
 :8306  
 :8307 :HERE FOR 3-OPERAND INTEGER AND BOOLE INSTRUCTIONS  
 :8308 :NAMELY ADDx3, SUBx3, BISx3, BICx3, XORx3 FOR x = B, W, L  
 :8309 :WHEN THE SECOND SPECIFIER IS MEMORY OR SHORT LITERAL  
 :8310  
 :8311 34A: :-----:  
 :8312 :D\_D[INST.DEP]Q, :DO THE OPERATION  
 :8313 :SET.CC(INST), :SET CONDITION CODES  
 :8314 :WRITE.DEST,J/WRD :GO WRITE DESTINATION BY SPEC 3  
 :8315  
 :8316 :HERE FOR MANY-OPERAND INSTRUCTIONS WHOSE EXECUTION STARTS ON D.FORK  
 :8317 :RE-DISPATCH THERE FOR FURTHER OPERATION  
 :8318  
 :8319  
 :8320 300: :-----:  
 :8321 :RC[T6]\_Q, :SAVE Q FOR LATER USE  
 :8322 :ID[T9]-D, :LIKEWISE D  
 :SUB/SPEC,J/ASPC.B :GO ON TO D.FORK

U 0349, C01D,C00C,0180,F804,4070,0062

U 034B, 081D,C00C,0180,F800,0070,0341

U 034A, F81D,C00F,01F0,F847,0070,0300

U 03C0, 0001,203F,E580,3DB0,0000,0400

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204]  
: P1W124.MCR 600,1204]  
: FORKS .MIC [600,1204]

J 2  
I-stream decode for 14-Jan-82  
MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124

Fiche 2 Frame J2

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I-stream decode forks : C-FORK for VAX Instructions

U 034D, 0001,203C,01E0,F800,0082,01FA

:8323 :HERE FOR ROTL, WITH THE COUNT IN Q AND THE SOURCE IN D  
:8324 34D:  
:8325 RRTL: SC Q,  
:8326 Q\_D  
:8327  
:8328  
:8329 D\_DAL.SC,  
:8330 B.FORK  
:8331  
:8332  
:8333 :HERE FOR ASHL, WITH THE COUNT IN Q AND THE SOURCE IN D  
:8334 34C:  
:8335 ASHL: SC Q.SXT[BYTE],  
:8336 Q\_0.  
:8337  
:8338 CLR\_SD&SS,  
:8339 D31?  
:8340  
:8341 =110 :D31=0  
:8342 EALU SC+K[.20],CLK.UBCC,  
:8343 RC[T0] Q,  
:8344 Q\_D,D\_DAL.SC,  
:8345 SC?,J7ASHL.1  
:8346  
:8347  
:8348 EALU SC+K[.20],CLK.UPCC,  
:8349 RC[T0] NOT.Q,  
:8350 Q\_D,D\_DAL.SC,  
:8351 SC?  
:8352  
:8353 =100 :SC\_EQL.0  
:8354 ASHL.1: ALU.D,N&Z ALU.V&C\_0,  
:8355 WRITE.DEST,J/WRD  
:8356  
:8357 :SC\_LSS.0  
:8358 D\_Q,  
:8359 Q\_RC[T0],  
:8360 EALU.N?,J/ASHL.4  
:8361  
:8362  
:8363 ID[T1] D,  
:8364 D\_RC[T0],  
:8365 Q\_Q.LEFT,SI/ZERO,  
:8366 SIGNS?,J/ASHL.2  
:8367  
:8368 :0\_LSS\_SC.LEQ.31  
:8369 :LEFT SHIFT. STORE RESULT TEMPORARILY  
:8370 :GET SIGNS FOR OVERFLOW TEST  
:8371 :DISCARD SIGN FROM SOURCE  
:8372 :BRANCH TO SET CONDITION CODE  
:8373 :SC\_GTR.31  
:8374 :RC[T0] 0,0,0,  
:8375 :N&Z ALU.V&C\_0,  
:8376 J/ASHL.8  
:8377 =  
:8378 :\*\*\*\*\*  
:8379 : \* Patch no. 067, PCS 01E7 trapped to WCS 118D \*  
:8380 :\*\*\*\*\*

U U1FA, FD00,003F,01F0,F847,0000,0200

U 034C, 0002,AD3C,01FF,F800,0082,0116

U 0116, 0D01,343C,75E0,F980,0014,81E4

U 0117, 0D01,3428,75E0,F980,0014,81E4

U 01E4, F001,003F,01F0,F847,0050,030C

U 01E5, 0C10,1238,01C0,F900,0000,0096

U 01E6, 0810,0D38,C5A8,3D00,0000,0234

U 01E7, 0003,003C,01F8,F980,0050,01A9

ZZ-ESOAA-124.0 : FORKS .MIC [600,1204]  
: P1W124.MCR 600,1204]  
: FORKS .MIC [600,1204]

MICR02 1L(03) I-stream decode for14-Jan-82  
I-stream decode forks : C-FORK for VAX Instructions

K 2

I-stream decode for14-Jan-82

14-Jan-82 15:30:16

VAX11/780 Microcode

Fiche 2 Frame K2

: PCS 01, FPLA 0E, WCS124

Sequence 229

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U 0234. 0D03,003C,C5F0,2C00,0050,01A9

:8376 :HERE FOR LEFT SHIFT  
:8377 :RESULT IS IN ID[T1], SOURCE IS IN Q, SHIFTED LEFT ONCE,  
:8378 : 32 COPIES OF SIGN ARE IN D, AND SHIFT AMOUNT (POSITIVE) IS IN SC  
:8379  
:8380 =100 :-----;D,EQL,0  
:8381 ASHL.2: ALU\_0(A),LONG,N&Z\_ALU.V&C\_0, ;CLEAR N, SET Z  
:8382 D\_DAL.SC, ;GATHER BITS SHIFTED INTO SIGN POSITION  
:8383 Q\_ID[T1],J,ASHQ.8 ;GET BACK RESULT FOR STORING

U 0236. 0D18,0038,C5F0,2C00,0050,01A9

:8384  
:8385 =110 :-----;D,GTR,0  
:8386 ALU\_K[.88],LONG,N&Z\_ALU.V&C\_0, ;CLEAR N & Z (CONSTANT IRRELEVANT)  
:8387 D\_DAL.SC, ;GATHER BITS SHIFTED INTO SIGN POSITION  
:8388 Q\_ID[T1],J,ASHQ.8 ;GET BACK RESULT FOR STORING

U 0237. 0D03,0028,C5F0,2C00,0050,01A9

:8389 :-----;D,LSS,0  
:8390 ALU\_-1,LONG,N&Z\_ALU.V&C\_0, ;SET N, CLEAR Z  
:8391 D\_DAL.SC, ;GATHER BITS SHIFTED INTO SIGN POSITION  
:8392 Q\_ID[T1],J,ASHQ.8 ;GET BACK RESULT FOR STORING

:8393  
:8394 :;END OF CONSTRAINT FOR BEN/SIGNS

:8395 :HERE ON RIGHT SHIFTS

:8396 :D CONTAINS THE SOURCE, Q IS FULL OF SIGN BITS,  
:8397 : AND SC HAS THE SHIFT COUNT, WHICH IS NEGATIVE

:8398 :-----  
:8399 :-----

:8400 :-----  
:8401 :-----

:8402 :-----  
:8403 :ASHL.4: D\_DAL.SC, ;SHIFT SOURCE

:8404 J,ASHL.1 ;GO SET CONDITION CODES FROM RESULT

:8405 :-----  
:8406 :-----

:8407 :-----  
:8408 :-----

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U 0096. 0D00,003C,0180,F800,0000,01E4

:8409 :-----;EALU N=0  
:8410 ASHL.4: D\_DAL.SC, ;SHIFT SOURCE

:8411 J,ASHL.1 ;GO SET CONDITION CODES FROM RESULT

U 009E. FC01,203F,01F0,F847,0050,0300

:8412 :-----;EALU N=1 (COUNT .LSS. -32)  
:8413 D\_Q, ;RETURN SIGN BITS AS RESULT

:8414 ALU\_Q,N&Z\_ALU.V&C\_0, ;SET PSL CC ACCORDINGLY

:8415 WRITE.DEST,J,WRD ;STORE

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame L2 Sequence 230  
 : P1WT24.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCST24 Page 229  
 : FORKS .MIC [600,1204] I-stream decode forks : C-FORK for VAX Instructions

L 2

:8409 :HERE FOR ASHQ, WITH THE COUNT IN Q AND THE HIGH-ORDER LONGWORD OF SOURCE IN D  
 :8410 :RC[T0] AND ID[T0] ARE USED TO KEEP COPIES OF THE SIGN BITS  
 :8411 :RC[T1] HAS THE LOW-ORDER SOURCE, AND ID[T1] HAS THE HIGH-ORDER SOURCE  
 :8412  
 :8413 343:  
 :8414 ASHQ: SC Q,SXT[BYTE], :PUT COUNT IN SC  
 :8415 ID[T1]\_D, :SAVE HIGH-ORDER SOURCE  
 :8416 Q\_0, :TENTATIVE POSITIVE SIGN TO Q  
 :8417 STATE K[.88]. :SET STATE 3, NO OVERFLOW YET  
 :8418 CLR SD&SS, :EASE LATER EALU BRANCHES  
 :8419 D31?  
 :8420  
 :8421 =110 :D31=0  
 :8422 SC SC+K[.20],CLK,UBCC, :EALU N WILL SET IF SC .LSS. -32  
 :8423 RC[T0] Q, :REPLICATE SIGN (POS) TO TO  
 :8424 Q\_D,D\_0, :HIGH SOURCE TO Q, SIGN TO D  
 :8425 SC?,J7ASHQ.1 :TEST RANGE OF SC  
 :8426  
 :8427 :D31=1  
 :8428 SC SC+K[.20],CLK,UBCC, :TEST FOR COUNT .LSS. -32  
 :8429 Q\_D, :HIGH SOURCE TO Q  
 :8430 D\_NOT\_Q, :MAKE D ALL NEGATIVE SIGN BITS  
 :8431 RC[T0]\_ALU, :PUT NEGATIVE SIGN IN TO, TOO  
 :8432 SC?  
 :8433 :TEST RANGE OF COUNT IN SC  
 :8434 =100 ASHQ.1: SC .EQ. 0 (NO SHIFT)  
 :8435 D\_RC[T1], :LOW RESULT TO D  
 :8436 NZ\_ALU.V&C\_0, :SET Z TENTATIVELY FROM LOW PART  
 :8437 SIGNS?,J/ASHQ.6 :SINCE THIS MAY BE A LEFT SHIFT BY A  
 :8438 : MULTIPLE OF 32, CHECK FOR OVERFLOW  
 :8439  
 :8440 ASHQ.2: SC .LSS. 0 (RIGHT SHIFT)  
 :8441 D\_DAL.SC, FE SC-K[.20], :HIGH RESULT TO D (IF SC IN RANGE)  
 :8442 EALU.N?,J/ASHQ.4 :TEST FOR HUGE SHIFT AMOUNT  
 :8443  
 :8444 :0 .LSS. SC .LEQ. 31  
 :8445 ID[T0]\_D, :SAVE SIGNS AGAIN  
 :8446 D\_RC[T1], :GET LOW SOURCE  
 :8447 Q\_0, :AND ZEROS TO SHIFT IN  
 :8448 J7ASHQ.7 :GO SHIFT LEFT  
 :8449  
 :8450 :SC .GTR. 31  
 :8451 ALU\_D\_XOR\_Q, :CALCULATE DIFF OF HIGH SRC FROM SIGN  
 :8452 CLK,UBCC,LONG, :SET Z IF NO OVERFLOW  
 :8453 SC\_SC-K[.40] :REDUCE SHIFT AMOUNT BY 32  
 :8454 : (COMPENSATING FOR EXTRA ADD ABOVE)  
 :8455 =END OF SC TEST

:E456 ;HERE WITH SHIFT COUNT GREATER OR EQUAL TO 32  
 :8457  
 :8458  
 :8459  
 :8460  
 :8461  
 :8462  
 :8463  
 U 021E, 0810,0138,75E0,F908,0104,61C8 Q\_D, :SAVE SIGNS  
 :D\_RC[T1], :GET LOW SOURCE  
 :FE\_K[.20], :PREPARE TO RE-OFFSET SC  
 :Z? :DID OVERFLOW OCCUR?  
 :  
 :8464 =0 :-----:Z=0, OVERFLOW  
 :8465 STATE\_0(A) :CLEAR STATE 3, TO INDICATE OVERFLOW  
 :8466  
 :8467 :-----:Z=1, NO OVERFLOW  
 :8468 :ID[T1].D,Q\_D, :SAVE LOW SOURCE AS HIGH  
 :8469 :RCC[1].0, :CLEAR LOW SOURCE  
 :8470 :D\_Q, :GET SIGNS BACK INTO D  
 :8471 :SC SC+FE, :RE-OFFSET SC BY 32  
 :8472 :SC?.J/ASHQ.1 :GO AROUND AGAIN  
 :8473  
 :8474 ;HERE ON RIGHT SHIFTS  
 :8475 ; Q CONTAINS THE HIGH PART OF THE SOURCE, D HAS THE HIGH RESULT  
 :8476 ; SC HAS THE SHIFT COUNT, WHICH WAS ORIGINALLY NEGATIVE.  
 :8477 ; BUT HAS HAD 32 ADDED TO IT. WE ARE BRANCHING ON THE SIGN OF THAT ADDITION  
 :8478  
 :8479 =011\* :-----:EALU N=0  
 :8480 ASHQ.4: :ID[T1].D, :SAVE HIGH RESULT  
 :8481 :D\_RC[TT].SC\_FE, :GET LOW SOURCE, RESTORE NEG SHIFT CT  
 :8482 :J7ASHQ.5 :GO GET LOW RESULT  
 :  
 :8483 :-----:EALU N=1 (COUNT .LSS. -32)  
 :8484 :RC[T1].Q :MOVE HIGH SOURCE ONTO LOW SOURCE  
 :  
 :8485 :-----:GET SIGNS FOR HIGH WORD  
 :8486 :Q\_RC[T0], :AND FOR SIGNS  
 :8487 :D\_RC[T0], :SEE IF COUNT IS NOW REASONABLE  
 :8488 :SC SC+K[.20].CLK.UBCC, :AND LOOP UNTIL IT IS.  
 :8489 :  
 :8490 :  
 :8491 :  
 U 01C9, 0C03,143C,C5E0,3D88,0080,8264  
 U 00B6, 0810,0038,C580,3D08,0081,0251  
 U 00BE, 0C01,203C,0180,F988,0000,0222  
 U 0222, 0810,0038,75C0,F900,0094,8265

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FORKS .MIC [600,1204] I-stream decode forks : C-FORK for VAX Instructions

N 2

Fiche 2 Frame N2 Sequence 232  
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U 0251, 0D00,003C,C5F0,2C00,0000,0254	:8492 :HERE ON RIGHT SHIFTS WHEN THE SHIFT COUNT HAS BEEN REDUCED TO LESS :8493 : THAN 32. THE HIGH RESULT HAS BEEN GENERATED AND SAVED IN ID[T1], Q HAS :8494 : THE HIGH SOURCE, AND D HAS THE LOW SOURCE.
U 0254, 0001,003C,0180,F800,0050,0272	:8496 :----- :8497 ASHQ.5: D_DAL.SC, :GET LOW RESULT IN D :8498 Q_ID[T1] :AND HIGH RESULT :8499 :----- :8500 :----- :8501 ALU.D,N&Z_ALU.V&C_0. :TEST LOW ORDER FOR Z :8502 J/ASHQ.6 :RE-ARRANGE FOR STORAGE :8503 :----- :8504 :ENTER HERE WITHOUT BRANCH ON RIGHT SHIFTS. ON SHIFTS OF 0 PLACES, COME HERE :8505 : FROM ASHQ.1 BRANCHING ON SIGNS OF D AND Q, WHICH ARE IDENTICAL. :8506 : ON LEFT SHIFTS BY A MULTIPLE OF 32 PLACES, ENTER FROM ASHQ.1, TESTING THE :8507 : SIGN OF THE ORIGINAL SOURCE IN D31, AND THE SIGN OF THE SHIFTED RESULT :8508 : IN Q31. IF THEY ARE NOT EQUAL, WE MUST SET OVERFLOW. :8509 :----- :8510 =010 ASHQ.6: :Q31 & D31 BOTH 0 :8511 RC[T1].Q, :SAVE HIGH PART FOR LATER STORE :8512 N_AMX.Z_TST, :SET N FROM HIGH, 'AND' Z WITH LOW :8513 STATE3?,J/ASHQ.6A :WAS THERE AN EARLIER OVERFLOW? :8514 :----- :8515 RC[T1].Q, :Q31 =0, D31 =1 :8516 N_AMX.Z_TST, :SAVE HIGH PART FOR LATER STORE :8517 Q_D, :SET N FROM HIGH, 'AND' Z WITH LOW :8518 J/ASHQ.7A :COPY LOW ORDER LONGWORD :8519 :GO SET OVERFLOW :8520 :----- :8521 RC[T1].Q, :Q31 =1, D31 =0 :8522 N_AMX.Z_TST, :SAVE HIGH PART FOR LATER STORE :8523 Q_D, :SET N FROM HIGH, 'AND' Z WITH LOW :8524 J/ASHQ.7A :COPY LOW ORDER LONGWORD :8525 :GO SET OVERFLOW :8526 :----- :8527 RC[T1].Q, :Q31 & D31 BOTH 1 :8528 N_AMX.Z_TST, :SAVE HIGH PART FOR LATER STORE :8529 STATE3?,J/ASHQ.6A :SET N FROM HIGH, 'AND' Z WITH LOW :8530 :WAS THERE AN EARLIER OVERFLOW? :8531 :----- :8532 =0*** ASHQ.6A:SET.V, :STATE 3=0 (OVERFLOW EARLIER) :8533 WRITE.DEST,J/WRD :NOTE OVERFLOW IN PSL :8534 :----- :8535 :***** :8536 : * Patch no. 016, PCS 0181 trapped to WCS 1153 * :8537 :***** :8538 :----- :8539 :----- :8540 U 0189, F000,003F,01F0,F847,0020,0300 :STATE 3=1 (NO OVERFLOW) :8541 WRITE.DEST,J/WRD

ZZ-ES0AA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame B3 Sequence 233  
 ; P1W124.MCR 600,1204] MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 232  
 ; FORKS .MIC [600,1204] I-stream decode forks : C-FORK for VAX Instructions

:8542 :HERE FOR LEFT SHIFT  
 :8543 : D HAS THE LOW SOURCE, Q IS ZERO,  
 :8544 : AND SHIFT AMOUNT (POSITIVE) IS IN SC, WITH 32 ADDED TO IT.  
 :8545  
 :8546  
 :8547 ASHQ.7: D\_DAL.SC, ;GET LOW PART OF RESULT  
 :8548 Q\_D, ;SAVE LOW SOURCE IN Q  
 :8549 SC\_SC-K[.40] ;MAKE SHIFT COUNT NEGATIVE  
 :8550  
 :8551  
 :8552 RC[T2] D, ;SAVE LOW RESULT  
 :8553 N&Z\_ALU.V&C\_0, ;SET TENTATIVE Z  
 :8554 D\_Q, ;LOW SOURCE TO D  
 :8555 Q\_ID[T1] ;HIGH SOURCE TO Q  
 :8556  
 :8557 D\_DAL.SC ;GET HIGH PART OF RESULT  
 :8558  
 :8559  
 :8560 RC[T1] D, ;SAVE HIGH RESULT  
 :8561 N\_AMX.Z\_TST, ;SET CONDITION CODES FROM THAT  
 :8562 D\_Q, ;HIGH SOURCE TO D  
 :8563 Q\_ID[T0], ;SIGNS TO Q  
 :8564 SC\_SC+1 ;PREPARE TO TEST BITS SHIFTED INTO 31  
 :8565  
 :8566  
 :8567 D\_DAL.SC, ;GET BITS DISCARDED FROM HIGH WORD  
 :8568 Q\_RC[T2], ;GET BACK LOW RESULT  
 :8569 STATE3? ;DID WE SEE OVERFLOW IN LONG SHIFT?  
 :8570  
 :8571  
 :8572 =0\*\*\* ASHQ.7A: D\_Q, ;STATE3=0, LONG SHIFT SAW OVERFLOW  
 :8573 SET\_V, ;READY LOW RESULT  
 :8574 WRITE\_DEST,J/WRD ;NOTE OVERFLOW  
 :8575 ;STORE IT BY FINAL SPECIFIER  
 :8576  
 :8577 : \*\*\*\*\*  
 :8578 : \* Patch no. 017, PCS 01A1 trapped to WCS 1154 \*  
 :8579 : \*\*\*\*\*  
 :8580  
 :8581 ASHQ.8: ALU\_D.XOR.RC[T0], ;STATE3=1, NO C/ERFLOW DETECTED  
 :8582 SET\_CC(INST), ;WERE BITS DISCARDED ALL SIGNS?  
 :8583 D\_Q, ;SET V IF NOT  
 :8584 J7SPEC ;READY LOW RESULT FOR STORING  
 :8585 ;GO STORE ACCORDING TO SPECIFIER

ZZ-ES0AA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82  
 ; P1W124.MCR 600,1204] MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124  
 ; FORKS .MIC [600,1204] I-stream decode forks : [-FORK for VAX Instructions

C 3

Fiche 2 Frame C3

Sequence 234

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:8586 ;HERE FOR AOBLLSS, AOBLEQ
:8587 ; WITH THE LIMIT IN Q, AND THE INDEX IN D
:8588
:8589 346: -----
:8590 AOB: D D+K[.1], :INCREMENT THE INDEX
:8591 SET.CC(INST) :SET CC FROM IT
:8592
:8593 -----
:8594 ALU_D-Q, :COMPARE INDEX TO LIMIT
:8595 CLK_UBCC, :PREPARE TO BRANCH ON RESULT
:8596 Q_IB.BDEST, :GET BDEST
:8597 PC PC+1,
:8598 IB.TEST?
:8599
:8600 =00
:8601 AOB.1: CALL.J/IB.TBR
:8602
:8603 -----
:8604 CALL.J/IB.ERR
:8605
:8606 -----
:8607 Q_IB.BDEST,
:8608 IB.TEST?,J/AOB.1
:8609
:8610 -----
:8611 CACHE_D[LONG], :STORE INDEX, UPDATED
:8612 Q_Q+PC, :COMPUTE BRANCH DESTINATION
:8613 CLR_IB0-1, :DISCARD THIS OPCODE & BDEST
:8614 PC PC+1, :AND POINT PC TO NEXT
:8615 ALU? :SHOULD WE BRANCH?
:8616
:8617 =;END OF IB.TEST
:8618
:8619 =0001
:8620 AOB.2: IRD :N=0, Z=0, IRO=0
:8621
:8622 IRD :N=0, Z=0, IRO=1
:8623
:8624
:8625 IRD :N=0, Z=1, IRO=0 (AOBLSS)
:8626
:8627
:8628
:8629 PC&VA_Q,FLUSH.IB, :N=0, Z=1, IRO=1 (AOBLEQ)
:8630 J/IB.FILL :BRANCH
:8631
:8632
:8633 PC&VA_Q,FLUSH.IB, :N=1
:8634 J/IB.FILL :BRANCH
:8635
:8636
:8637 PC&VA_Q,FLUSH.IB, :N=1
:8638 J/IB.FILL :BRANCH
:8639
:8640 =;END OF ALU.CC TEST

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ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204]  
; P1W124.MCR 600,1204]  
; FORKS .MIC [600,1204]

I-stream decode for14-Jan-82  
MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124

D 3 Fiche 2 Frame D3

Sequence 235

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I-stream decode forks : C-FORK for VAX Instructions

U 03C4, 0002,E03D,0180,F980,0000,037E

:8641 :HERE FOR ACBB, ACBW, ACBL  
:8642 : FIRST OPERAND (LIMIT) IS IN Q, SECOND OPERAND (ADDEND) IS IN D

:8643  
:8644 3C4: -----  
:8645 ACB: RC[T0] Q.SXT[INST.DEP], :CALL SITE FOR INDEX SPECIFIER EVAL  
:8646 CALL,J7SPEC :SAVE LIMIT, SIGN EXTENDED  
:8647 :GO EVALUATE INDEX SPECIFIER

U 03D4, 7002,EB3D,01F0,F98D,0000,0478

:8648 3D4: -----  
:8649 RC[T1] Q.SXT[INST.DEP], :RETURN HERE WITH MEMORY OPERAND  
:8650 Q\_IB.BDEST, :SAVE ADDEND, SIGN EXTENDED  
:8651 PC\_PC+2 :GET BDEST FROM IB  
:8652 IB.TEST?,CALL,J/ACB.8 :STEP PC PAST WORD DISPLACEMENT  
:8653 :GO WAIT FOR IT IF NECESSARY

U 03D5, D811,C014,0180,F800,0070,0280

:8654 3D5: -----  
:8655 D\_D+LC, :INDEX IS IN MEMORY  
:8656 C[R\_IB].SPEC, :INDEX + ADDEND  
:8657 SET.CC(INST), :DISCARD 2ND BYTE OF BDEST  
:8658 J/ACB.1 :SET PSL CC FROM SUM  
:8659 :GO STORE BACK IN MEMORY

U 03D6, 7002,EB3D,01F0,F98D,0000,0478

:8660 3D6: -----  
:8661 RC[T1] Q.SXT[INST.DEP], :RETURN HERE WITH REGISTER OPERAND  
:8662 Q\_IB.BDEST, :SAVE ADDEND, SIGN EXTENDED  
:8663 PC\_PC+2, :GET BDEST FROM IB  
:8664 IB.TEST?,CALL,J/ACB.8 :STEP PC PAST WORD DISPLACEMENT  
:8665 :GO WAIT FOR IT IF NECESSARY

U 03D7, D811,C014,0180,F8D8,0070,02A9

:8666 3D7: -----  
:8667 D\_D+LC, :INDEX IS IN A REGISTER  
:8668 C[R\_IB].SPEC, :INDEX + ADDEND  
:8669 R(PRN) ALU, :DISCARD 2ND BYTE OF BDEST  
:8670 SET.CC(INST) :STORE AS FINAL RESULT

:8671 :END OF SUBROUTINE CONSTRAINT STARTED AT ACB

U 02A9, 0000,1B3C,0180,F900,0000,00C7

:8672 :-----  
:8673 LC RC[T0], :RECOVER LIMIT  
:8674 ALU.N?,J/ACB.2 :TEST SIGN OF ADDEND

U 02B0, 0000,DB3C,0180,3100,0000,00C7

:8675 ACB.1: CACHE\_D[INST.DEP], :STORE UPDATED INDEX  
:8676 LC RC[T0], :GET LIMIT BACK  
:8677 ALU.N? :TEST SIGN OF ADDEND

U 00C7, 0011,C008,0180,F800,0010,02D0

:8678 ACB.2: -----  
:8679 ALU\_D-1  
:8680 DT/INST.DEP,CLK.UBCC, :ADDEND .GEQ. 0  
:8681 J/ACB.3 :COMPARE INDEX TO LIMIT  
:8682 :-----  
:8683 \* Patch no. 060, PCS 00C7 trapped to WCS 1186 \*  
:8684 :-----  
:8685 DT/INST.DEP,CLK.UBCC :REF T OF COMPARE TO ALU N  
:8686 J/ACB.3 :GO TEST IT  
:8687 :-----

:8688 :\*\*\*\*\*  
:8689 : \* Patch no. 060, PCS 00C7 trapped to WCS 1186 \*  
:8690 :\*\*\*\*\*  
:8691 :-----

U 00CF, 0011,C000,0180,F800,0010,02C6

:8692 ALU\_D-LC, :ADDEND .LSS. 0  
:8693 DT/INST.DEP,CLK.UBCC :COMPARE INDEX TO LIMIT  
:8694 :-----

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204]  
; P1W124.MCR 600,1204]  
; FORKS .MIC [600,1204]

I-stream decode for14-Jan-82  
MICR02 1L(03) 14-Jan-82 15:30:16  
I-stream decode forks : C-FORK for VAX Instructions

E 3

Fiche 2 Frame E3

Sequence 236

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U 02C6, C015,3B14,01C0,F804,4000,0367

U 0367, 2001,203C,0180,F801,4200,00AB

U 036F, F80C,003B,01F1,F857,1398,6000

U 02D0, C015,3B14,01C0,F804,4000,0497

U 0497, F80C,003B,01F1,F857,1398,6000

U 049F, 2001,203C,0180,F801,4200,00AB

U 0478, 0000,003D,0180,F800,0000,0E6E

U 0479, 0000,003D,0180,F800,0000,0880

U 047A, 7000,0B3C,01F0,F800,0000,0478

U 047B, D010,003A,0180,F908,0010,0001

;8695 ;HERE FOR ACB, AFTER COMPARING THE UPDATED INDEX TO THE LIMIT  
;8696  
;8697 ;-----;  
;8698 Q\_Q+PC,  
;8699 CLR.IB.OPC,  
;8700 PC PC+1,  
;8701 ALU.N?  
;8702  
;8703 =0111 ;-----;  
;8704 PC&VA\_Q,FLUSH.IB,J/IB.FILL  
;8705  
;8706 ;-----;  
;8707 IRD  
;8708  
;8709  
;8710 ACB.3: ;-----;  
;8711 Q\_Q+PC,  
;8712 CLR.IB.OPC,  
;8713 PC PC+1,  
;8714 ALU.N?  
;8715  
;8716 =0111 ;-----;  
;8717 IRD  
;8718  
;8719 ;-----;  
;8720 PCRVA\_Q,FLUSH.IB,J/IB.FILL  
;8721  
;8722  
;8723 ;HERE IS SUBROUTINE USED BY ACB TO GET BRANCH DISPLACEMENT  
;8724  
;8725 =00 ACB.8: ;-----;  
;8726 CALL,J/IB.TBR  
;8727  
;8728 ;-----;  
;8729 CALL,J/IB.ERR  
;8730  
;8731  
;8732 Q\_IB.BDEST,  
;8733 IB.TEST?,J/ACB.8  
;8734  
;8735  
;8736 ALU\_RC[T1],CLK.UBCC,  
;8737 CLR.IB.SPEC,  
;8738 RETURN1  
;-----;  
;TRY AGAIN TO GET BDEST  
;LOOP WAITING  
;-----;  
;GET ADDEND TO LC, TEST ITS SIGN  
;DISCARD 1ST BYTE OF BDEST

F 3

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame F3 Sequence 237  
 : PTW124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 236  
 ; FORKS .MIC [600,1204] I-stream decode forks : C-FORK for VAX Instructions

```

:8739 ;HERE FOR BBS, BBC, BBSS, BBCS, BBSC, BBCC, BBSSI, BBCCI
:8740 ; WHEN BIT TESTED IS NOT IN A REGISTER
:8741 ; D CONTAINS THE BASE ADDRESS, Q HAS THE BIT POSITION
:8742
:8743 345: -----
:8744 BB: RC[T0]_D ;SAVE BASE OF BIT TABLE
:8745
:8746 -----
:8747 SC Q, ;LOW BITS OF POSITION TO SC
:8748 D_Q.RIGHT2, ;DISCARD BITS OF POSITION
:8749 Q_IB.BDEST,
:8750 PC_PC+1,
:8751 IB.TEST?
:8752
:8753 ; *****
:8754 ; * Patch no. 062, PCS 02EE trapped to WCS 1188 *
:8755 ; *****
:8756
:8757 =00
:8758 BB.1: -----;
:8759
:8760 -----;
:8761 CALL,J/IB.ERR
:8762
:8763 -----;
:8764 Q_IB.BDEST
:8765 IB.TEST?,J/BB.1
:8766
:8767
:8768 CLR.IB.SPEC. ;DISCARD BDEST FROM IB BYTE1
:8769 D_D.RIGHT ;POSITION NOW RIGHT 3 PLACES
:8770 ALU Q.OXT[BYTE], CLK.UBCC, ;TEST BDEST FOR 0 (HACK CASE)
:8771 LC_RC[T0], ;READY BASE ADDRESS
:8772 SC_SC.ANDNOT.K.[FFF8] ;GET ONLY BIT POSITION IN BYTE
:8773
:8774 =;END OF IB.TEST
:8775
:8776 FO.PA.62:
:8777
:8778 VA_D+LC, ;COMPUTE BYTE ADDRESS OF BIT TO TEST
:8779 IR2-1? ;WHAT KIND OF REFERENCE?
:8780
:8781 =*00 -----;NO MODIFICATION
:8782 D[BYTE]_CACHE, Z?, J/BB.2
:8783
:8784 -----;SET
:8785 D[BYTE]_CACHE.WCHK, Z?, J/BB.2
:8786
:8787 -----;CLEAR
:8788 D[BYTE]_CACHE.WCHK, Z?, J/BB.2
:8789
:8790 -----;INTERLOCK
:8791 D[BYTE]_CACHE.LK, Z?, J/BB.2 ;

```

ZZ-ES0AA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame G3 Sequence 238  
 : PTW124.MCR 600,1204] MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 237  
 : FORKS .MIC [600,1204] I-stream decode forks : C-FORK for VAX Instructions

G 3

```

:8792 ;HERE FOR BB GROUP, WITH BYTE TO BE TESTED IN D,
:8793 ; AND BIT NUMBER OF BIT TO TEST IN SC
:8794
:8795 =0 -----;BDEST_NE_0
:8796 BB.2: ALU_D.ANDNOT.MASK. ;TEST SELECTED BIT
:8797 CLK.UBCC,
:8798 IR2-1?, J/BB.3
:8799
:8800 -----;BDEST = 0
:8801 D_D[INST.DEP]MASK. ;DON'T TEST - JUST ALTER
:8802 C[R.IB.OPC, PC_PC+1. ;GET RID OF OPCODE SPECIFIER
:8803 IR2-1? ;CHECK REFERENCE TYPE
:8804
:8805 =*00 -----;NO MODIFICATION
:8806 IRD ;RATHER POINTLESS INSTRUCTION, WHAT?
:8807
:8808 -----;SET
:8809 CACHE_D[BYTE], J/IRD ;WRITE BYTE AND FALL THROUGH
:8810
:8811 -----;CLEAR
:8812 CACHE_D[BYTE], J/IRD ;WRITE BYTE AND FALL THRU
:8813
:8814 -----;INTERLOCK
:8815 CACHE_D[BYTE].LK, J/IRD ;WRITE BYTE, RELEASE INTLK & FALL THRU
:8816
:8817
:8818 =*00 -----;NO MODIFICATION
:8819 BB.3: Q_Q+PC, ;COMPUTE BRANCH ADDR
:8820 C[R.IB.OPC, ;DISCARD OPCODE SO NEXT IS READY
:8821 PC_PC+1, ;POINT PC PAST IT
:8822 AL0?, J/BB.5 ;DECIDE WHETHER TO BRANCH
:8823
:8824 -----;SET
:8825 D_D[INST.DEP]MASK. ;DO IT TO IT
:8826 J7BB.4
:8827
:8828 -----;CLEAR
:8829 D_D[INST.DEP]MASK. ;DO IT TO IT
:8830 J7BB.4
:8831
:8832 -----;INTERLOCK
:8833 D_D[INST.DEP]MASK
:8834
:8835 -----;WRITE BACK, CLEARING THE LOCK
:8836 CACHE_D[BYTE].LK, ;WRITE BACK, CLEARING THE LOCK
:8837 Q_Q+PC,
:8838 C[R.IB.OPC,
:8839 PC_PC+1,
:8840 AL0?, J/BE.5
:8841
:8842
:8843 BB.4: CACHE_D[BYTE], ;WRITE BACK
:8844 Q_Q+PC,
:8845 C[R.IB.OPC,
:8846 PC_PC+1,
  
```

ZZ-ES0AA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame H3 Sequence 239  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 238  
 : FORKS .MIC [600,1204] I-stream decode forks : C-FORK for VAX Instructions

U 0322, C015, BB14, 01C0, 3004, 4000, 02E9	:8847	ALU?
	:8848	
U 02E9, 2001, 203C, 0180, F801, 4200, 00AB	:8849 =1001	-----;Z=0, BBS
	:8850 BB.5:	PC&VA_Q, FLUSH.IB,J/IB.FILL ;BRANCH
	:8851	
U 02EB, F80C, 003B, 01F1, F857, 139B, 6000	:8852	-----;Z=0, BBC
	:8853	IRD
U 02ED, F80C, 003B, 01F1, F857, 139B, 6000	:8854	
	:8855	-----;Z=1, BBS
	:8856	IRD
	:8857	
U 02EF, 2001, 203C, 0180, F801, 4200, 00AB	:8858	-----;Z=1, BBC
	:8859	PC&VA_Q, FLUSH.IB,J/IB.FILL

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] I-stream decode for14-Jan-82 Fiche 2 Frame I3 Sequence 240  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 239  
 ; FORKS .MIC [600,1204] I-stream decode forks : (-FORK for VAX Instructions

;8860 ;HERE FOR CASEB AND CASEW  
 ;8861 ; THE FIRST OPERAND (SELECTOR) IS IN Q, THE SECOND (BASE) IS IN D  
 ;8862  
 ;8863 383: ;-----;CALL SITE FOR LIMIT SPECIFIER EVAL  
 ;8864 CASEB:  
 ;8865 CASEW: D\_Q-D, ;COMPUTE TMP AS SELECTOR-BASE  
 ;8866 CALL,J/SPEC ;GO EVALUATE LIMIT SPECIFIER  
 ;8867  
 ;8868 393: ;-----;RETURN HERE FROM SPECIFIER EVALUATION  
 ;8869 ALU\_D-Q-1, ;COMPARE TMP TO LIMIT  
 ;8870 SET.CC(INST) ;SET PSL CC ACCORDINGLY  
 ;8871  
 ;8872  
 ;8873 Q\_Q.OXT[INST.DEP].LEFT, ;MULTIPLY TMP BY 2 FOR ADDRESSING BDEST  
 ;8874 PSL.CC? ;DECIDE WHETHER TO BRANCH  
 ;8875  
 ;8876 =10\*0  
 ;8877 F0.ABS.28:  
 ;8878 ;-----;Z=0, C=0 (TMP GTRU LIMIT)  
 ;8879 Q\_D.Q.OXT[INST.DEP]+K(.1).LEFT. ;(LIMIT+1)\*2 GIVES LENGTH OF BDEST LIST  
 ;8880 J7BR ;BRANCH PAST THE LIST  
 ;8881  
 ;8882 ;-----;Z=0, C=1 (TMP LSSU LIMIT)  
 ;8883 VA\_Q+PC,J/CASE.1 ;GET ADDRESS OF SELECTED BDEST  
 ;8884  
 ;8885 F0.ABS.2C:  
 ;8886 ;-----;Z=1, C=0 (TMP EQL LIMIT)  
 ;8887 VA\_Q+PC,J/CASE.1  
 ;8888  
 ;8889 =;END OF PSL.CC TEST

	:8890	;HERE FOR CASEL	
	:8891	; THE FIRST OPERAND (SELECTOR) IS IN Q. THE SECOND (BASE) IS IN D	
	:8892		
	:8893	30E: -----	;CALL SITE FOR LIMIT SPEC EVALUATION
U 030E, 081D,2001,0180,F800,0000,037E	:8894	CASEL: D_Q-D,	;COMPUTE TMP AS SELECTOR-BASE
	:8895	CALL.J/SPEC	;GO EVALUATE LIMIT SPECIFIER
	:8896		
	:8897	31E: -----	;RETURN HERE FROM SPECIFIER EVALUATION
U 031E, 001D,C008,01A8,F800,0070,036B	:8898	ALU_D-Q-1,	;COMPARE TMP TO LIMIT
	:8899	SET.CC(INST),	;SET PSL CC ACCORDINGLY
	:8900	Q_Q.LEFT	;SHIFT TMP FOR ADDRESSING BDEST LIST
	:8901		
U 036B, 0015,3A14,0180,F800,0200,0138	:8902	-----	
	:8903	VA_Q+PC,	;ADDRESS SELECTED BDEST
	:8904	PSE.CC?	;DECIDE HOW TO BRANCH
	:8905		
U 0138, 0039,0014,05C0,F800,0000,00CE	:8906	=10*0 -----	;Z=0, C=0 (TMP GTRU LIMIT)
	:8907	Q_D+K[.1].LEFT,	; (LIMIT+1)*2 GIVES LENGTH OF BDEST LIST
	:8908	J7BR	;BRANCH PAST THE LIST
	:8909		
U 0139, 0000,403C,0180,4000,0000,036D	:8910	-----	Z=0, C=1 (TMP LSSU LIMIT)
	:8911	DEWORD].CACHE,	;GET SELECTED BDEST
	:8912	J/CASE.2	
	:8913		
U 013C, 0000,403C,0180,4000,0000,036D	:8914	CASE.1: DEWORD].CACHE -----	Z=1, C=0 (TMP EQL LIMIT)
	:8915		;GET SELECTED BDEST
	:8916		
	:8917	=;END OF PSL.CC TEST	
	:8918		
	:8919		
U 036D, 2016,4014,0180,F801,4200,00AB	:8920	CASE.2: PC&VA_D.SXT[WORD]+PC,	;BRANCH TO SELECTED ROUTINE
	:8921	FLUSH_IB,J/IB.FILL	

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204]  
 : P1W124.MCR 600,1204]  
 : FORKS .MIC [600,1204]

MICR02 1L(03) I-stream decode for14-Jan-82  
 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 I-stream decode forks : C-FORK Specifier Evaluation Subroutine

U 0300, 0C00,003E,01E0,F800,0000,0010

U 0301, 0000,003C,0180,F800,0000,0001

U 0302, 0F01,203E,01E0,F990,0000,0010

U 0303, 0000,003C,0180,F800,0000,0001

U 0304, 0800,003E,01E0,F800,0000,0012

U 0324, C001,C03C,0180,F8DC,4000,0062

U 0305, 0000,003C,0180,F800,0000,0001

```
:8922 .TOC   "      I-stream decode forks : C-FORK Specifier Evaluation Subroutine"
:8923
:8924 ;Control passes to this point by "CALL,J/SPEC" or from any 'WRITE.DEST' state.
:8925 ;LA, LB = Register selected by bits <3:0> of IB byte 1
:8926 ;D = Result to be stored, if WRITE.DEST; otherwise returned in Q
:8927 ;Q = Instruction stream data, if any
:8928 ;If the specifier evaluated is of 'READ' or 'MODIFY' type, control returns
:8929 ;at the call site ored with 10, for literal and memory operands, or the
:8930 ;call site ored with 12 for register operands. If 'WRITE' type, control
:8931 ;passes to IRD to perform the next instruction.
:8932
:8933 300: ;-----
:8934 WRD:
:8935 C.FORK: D.Q,Q,D           :SHORT LITERAL
:8936 RETURN10                      :RETURN LITERAL IN D
:8937
:8938 301: ;-----
:8939 J/RSVMOD                     :RESERVED MODE
:8940
:8941 302: ;-----
:8942 RC[CT2] Q,                   :QUAD/DOUBLE SHORT LITERAL
:8943 Q,D,D,0,                     :RETURN OLD D IN Q, REST IS ZERO
:8944 RETURN10
:8945
:8946 303: ;-----
:8947 J/RSVMOD                     :RESERVED MODE
:8948
:8949 304: ;-----
:8950 Q,D,D,LA,                   :REGISTER, TO READ
:8951 RETURN12
:8952
:8953 324: ;-----
:8954 WRD.R: R(PRN)_D,DT/INST.DEP, :REGISTER, TO WRITE
:8955 CLR,IB,OPC                   :GO TO NEXT INSTR
:8956 PC,PC+1,J/IRD
:8957
:8958 305: ;-----
:8959 J/RSVMOD
```

L 3

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame L3 Sequence 243  
 : P1WT24.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 242  
 : FORKS .MIC [600,1204] I-stream decode forks : C-FORK Specifier Evaluation Subroutine

```

;8960 ;GENERAL SPECIFIER (C-FORK) EVALUATION, CONTINUED
;8961
;8962 306: -----
;8963     RCT2_LA, ;QUAD REGISTER, TO READ
;8964     Q_D
;8965
;8966 F0.ABS.36E:
;8967     -----
;8968     D_R(PRN+1), ;HIGH ADDRESS PART TO D
;8969     RETURN12
;8970
;8971 326: -----
;8972     R(PRN)_D ;QUAD REGISTER. STUFF LOW ADDRESS PART
;8973
;8974     -----
;8975     D_RCT1] ;GET HIGH ADDRESS PART
;8976
;8977     -----
;8978     R(PRN+1)_D, ;NOW STORE HIGH ADDRESS PART
;8979     CLR.IB.OPC
;8980     PC_PC+1,J/IRD
;8981
;8982 307: -----
;8983     J/R SVMOD
;8984
;8985 308: -----
;8986     C.DR: VA_LA, ;(R)
;8987     Q_D
;8988     DATA.TYPE?,J/C.M
;8989
;8990 309: -----
;8991     R(PRN)_LA+K[SP1.CON].RLOG, ;(R)+ UPDATE THE STACK POINTER
;8992     J/C.DR ;THEN LOAD UN-INCREMENTED ADDR
;8993
;8994 30A: -----
;8995     R(PRN)_LA-K[SP1.CON].RLOG, ;-(R) AUTO DECREMENT
;8996     VA_ALU, ; USE DECREMENTED ADDR
;8997     Q_D
;8998     DATA.TYPE?,J/C.M
;8999
;9000 30B: -----
;9001     VA_LA, ;@ (R)+ AUTO INCREMENT DEFERRED
;9002     Q_D ;SAVE DATA WHILE GETTING INDIRECT
;9003
;9004     ****
;9005     * Patch no. 054, PCS 030B trapped to WCS 117C *
;9006     ****
;9007
;9008 F. BS.394:
;9009     -----
;9010     D[LONG] CACHE,
;9011     R(PRN)_A+K[.4].RLOG, ;GET INDIRECT WORD
;9012     J/C.DF ;WHILE UPDATING REGISTER
;9013     ; THEN JOIN COMMON CODE

```

U 0306, 0000,003C,01E0,F990,0000,036E

U 036E, 0800,003E,0180,F860,0000,0012

U 0326, 0001,003C,0180,F8D8,0000,0375

U 0375, 0810,0038,0180,F908,0000,0392

U 0392, C001,003C,0180,F8E4,4000,0062

U 0307, 0000,003C,0180,F800,0000,0001

U 0308, 0000,083C,01E0,F800,0200,02D2

U 0309, 0018,0018,1580,F8D8,0000,0308

U 030A, 0018,0804,15E0,F8D8,0200,02D2

U 030B, 0000,003C,01E0,F800,0200,0394

U 0394, 0018,0018,1180,40D8,0000,03C7

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204]  
: P1W124.MCR 600,1204] MICRO2 1L(03) I-stream decode for 14-Jan-82

I-stream decode for 14-Jan-82  
14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124

Fiche 2 Frame M3 Sequence 244  
I-stream decode forks : C-FORK Specifier Evaluation Subroutine

Page 243

M 3

9013 ;GENERAL SPECIFIER (C-FORK) EVALUATION. CONTINUED  
9014  
9015 30C: -----  
9016 RCT7 LA.CTX. ;INDEX MODE, CONTEXT SHIFT INDEX  
9017 CALL,J7ASPC ;AND GO EVALUATE BASE OPERAND ADDRESS  
9018  
9019 36C: -----  
9020 D Q. ;RETURN HERE WITH BASE OPERAND ADDRESS  
9021 VA D+LC. ;RESTORE DATA TO BE STORED  
9022 DATA.TYPE?,J/C.M ;COMPUTE INDEXED ADDRESS  
9023 ;GET OR STORE NORMAL OR QUAD  
9024  
9025 30D: -----  
9026 VA Q+LB.PC. ;D(R) DISPLACEMENT MODE.  
9027 Q D. ;SAVE OLD D  
9028 CLR.IB.SPEC. ;DISCARD THE SPECIFIER  
9029 DATA.TYPE?,J/C.M ;GO GET THE OPERAND  
9030  
9031 30F: -----  
9032 Q D,VA Q+LB.PC. ;D(R) DISPLACEMENT DEFERED  
9033 CLR.IB.SPEC. ;DROP THE SPECIFIER  
9034 ; \*\*\*\*\*  
9035 ; \* Patch no. 055, PCS 030F trapped to WCS 117D \*  
9036 ; \*\*\*\*\*  
9037  
9038 F0.ABS.38E:  
9039  
9040 D[LONG]\_CACHE ;GET INDIRECT, GO USE IT AS ADDR  
9041  
9042  
9043 C.DF: VA D. ;USE POINTER AS ADDRESS  
9044 D Q. ;GET DATA TO STORE BACK TO D  
9045 DATA.TYPE?,J/C.M

ZZ-ESOAA-124 0 ; FORKS .MIC [600,1204]  
 : P1W124.MCR 600,1204]  
 : FORKS .MIC [600,1204]

MICRO2 1L(03) I-stream decode for14-Jan-82  
 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 I-stream decode forks : C-FORK Specifier Evaluation Subroutine

;S046 ;HERE ARE VARIANTS OF THE C-FORK ENTRY POINTS FOR R=PC  
 ;9047  
 ;9048 314: ;-----;  
 ;9049 J/RSVMOD ;PC REGISTER MODE  
 ;9050  
 ;9051 315: ;-----;  
 ;9052 J/RSVMOD ;ILLEGAL REGISTER MODE, R=PC  
 ;9053  
 ;9054 316: ;-----;  
 ;9055 J/RSVMOD ;PC QUAD REGISTER MODE  
 ;9056  
 ;9057 317: ;-----;  
 ;9058 J/RSVMOD ;ILLEGAL QUAD REGISTER MODE, R=PC  
 ;9059  
 ;9060 318: ;-----;  
 ;9061 J/RSVMOD ;(PC)  
 ;9062  
 ;9063 319: ;-----;  
 ;9064 D Q,Q,D, ;(PC)+ IMMEDIATE  
 ;9065 CLR,IB,SPEC,  
 ;9066 RETURN10 ;DONE  
 ;9067  
 ;9068 ;\*\*\*\*\*  
 ;9069 ; \* Patch no. 047, PCS 0319 trapped to WCS 116F \*  
 ;9070 ;\*\*\*\*\*  
 ;9071  
 ;9072 31A: ;-----;  
 ;9073 J/RSVMOD ;-(PC)  
 ;9074  
 ;9075 31B: ;-----;  
 ;9076 VA Q,Q,D, ;Q(PC)+ ABSOLUTE MODE  
 ;9077 CLR,IB,SPEC,  
 ;9078 DATA.TYPE?,J/C.M  
 ;9079  
 ;9080 31C: ;-----;  
 ;9081 J/RSVMOD ;INDEX MODE, R=PC  
 ;9082  
 ;9083 31D: ;-----;  
 ;9084 J/RSVMOD ;NESTED INDEX MODE, R=PC  
 ;9085  
 ;9086 31E: ;-----;  
 ;9087 R[C71] Q, ;QUAD IMMEDIATE  
 ;9088 Q,IB,DATA, ;GET SECOND PART INTO Q  
 ;9089 CLR,IB,COND,  
 ;9090 PC PC+4, ;PUSH PC PAST SECOND PART  
 ;9091 IB,TEST?,J/C.IQ  
 ;9092  
 ;9093 ;\*\*\*\*\*  
 ;9094 ; \* Patch no. 058, PCS 031F trapped to WCS 1184 \*  
 ;9095 ;\*\*\*\*\*

B 4

:9096 ;SPECIAL CFORK STATES  
 :9097  
 U 0387, 0000.003D,0180,F800,0000,0EE0 :9098 387: ;-----;HERE WE SHOULD NEVER GET  
 :9099 CALL,J/EH.US EQ ;;"UNUSED" LOCATION FOUND IN IB ROM  
 :9100  
 :9101 ; \*\*\*\*\*  
 :9102 ; \* Patch no. 046, PCS 0387 trapped to WCS 116E \*  
 :9103 ; \*\*\*\*\*  
 :9104  
 U 037C, 0000.003D,0180,F800,0000,0E64 :9105 37C: ;-----;IB HAD NO DATA BECAUSE OF  
 :9106 CALL,J/IB.TBM ;TB MISS. REFILL IT  
 :9107  
 U 037D, 0000.003D,0180,F800,0000,0B80 :9108 37D: ;-----;IB HAD NO DATA BECAUSE OF  
 :9109 CALL,J/IB.ERR ;ANY ERROR. FIND OUT WHAT HAPPENED  
 :9110  
 U 037E, F000,003F,01F0,F847,0000,0300 :9111 37E: ;-----;IB IS WAITING FOR DATA  
 :9112 SPEC: LAB\_R(SP1), ;STALL  
 :9113 Q\_IB.DATA,  
 :9114 CLR\_IB.COND,  
 :9115 PC PC+N,  
 :9116 MCT/ALLOW\_IB.READ,  
 :9117 SUB/SPEC,J/C.FORK  
 :9118  
 U 037F, 0000.003C,0180,F800,0000,04F8 :9119 37F: ;-----;HERE IF INTERRUPT REQUEST UP  
 :9120 J/INT.B ;GO BACKUP REGISTERS, SERVE INTERRUPT  
 :9121  
 :9122 ;HERE TO WRITE BACK THE RESULT OF AN INSTRUCTION WITH A MODIFY DESTINATION.  
 :9123 ; ASSIGNED AN ADDRESS ON CFORK BECAUSE MANY 2-OPERAND INSTRUCTIONS ARE  
 :9124 ; EXECUTED BY THE SAME CODE AS THE 3-OPERAND COUNTERPART, AND CONCLUDE WITH  
 :9125 ; THE WRITE.DEST OPERATION, WHICH EVALUATES THE THIRD SPECIFIER IN THE  
 :9126 ; 3-OPERAND FORM, AND COMES HERE FOR THE 2-OPERAND FORM.  
 :9127  
 :9128 341:  
 U 0341, C000,C03C,0180,3004,4000,0062 :9129 STORE: CACHE\_D.INST.DEP, ;STORE RESULT BY INSTR DATA TYPE  
 :9130 CLR\_IB.OPC ;MOVE NEXT INSTR INTO IB BYTE 0  
 :9131 PC\_PC+1,J/IRD ;DO NEXT INSTRUCTION  
 :9132  
 :9133 ;HERE IS THE SAME FUNCTION FOR QUAD/DOUBLE OPERATIONS  
 :9134  
 :9135 344:  
 U 0344, 0010,0038,0180,F938,0200,02D3 :9136 STOR.Q: VA\_RC[T7], ;RELOAD OPERAND ADDRESS, WHICH GOT  
 :9137 J/T.WQ ;INCREMENTED IN FETCHING OPERAND

C 4

ZZ-ESOAA-124.0 ; FORKS .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame C4 Sequence 247  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 246  
 ; FORKS .MIC [600,1204] I-stream decode forks : C-FORK Specifier Evaluation Subroutine

```

:9138  ;HERE FOR THE SECOND AND SUBSEQUENT STATES OFF C-FORK SUBROUTINE
:9139
:9140 =010 ;-----;GET HERE BY DATA.TYPE?
:9141 C.M: CACHE_D.INST.DEP, ;STORE RESULT
:9142 CLR.IB.OPC,PC_PC+1,J/IRD ;GO ON TO NEXT INSTR
:9143
:9144 ;-----;
:9145 C.WQ: CACHE_D.INST.DEP,J/C.WQ1 ;STORE QUAD/DBL RESULT,GO WRT 2nd PART
:9146
:9147 ;-----;
:9148 D_CACHEINST.DEP, ;GET MEMORY OPERAND
:9149 RETURN10 ;RETURN IT
:9150
:9151 ;-----;
:9152 D_CACHEINST.DEP ;GET FIRST PART OF QUAD OPERAND
:9153 =;END OF DATA.TYPE TEST
:9154
:9155 ;-----;
:9156 RCET2] D, ;PUT LOW ADDR PART AWAY
:9157 ID_D.SYNC, ;SEND IT TO ACCELERATOR
:9158 VA_VA+4 ;GET HIGH ADDR READY
:9159
:9160 ;-----;
:9161 D[LONG]_CACHE,RETURN10 ;GET HIGH ADDR PART
:9162
:9163 ;HERE TO COMPLETE WRITE OF QUAD/DOUBLE OPERAND
:9164
:9165 ;-----;
:9166 C.WQ1: D_RC[T1], ;GET HIGH-ADDRESS DATA
:9167 VA_VA+4 ;AND GO WRITE IT
:9168
:9169 ;-----;
:9170 STOR.L: CACHE_D[LONG],CLR.IB.OPC, ;STORE SECOND PART OF QUAD RESULT
:9171 PC_PC+1,J/IRD ;GO BACK TO IRD
:9172
:9173 ;HERE FOR QUAD/DOUBLE IMMEDIATE OPERANDS
:9174
:9175 =00
:9176 C.IQ: CALL,J/IB.TBM
:9177
:9178 ;-----;
:9179 CALL,J/IB.ERR
:9180
:9181 ;-----;
:9182 Q_IB.DATA,CLR.IB2-5,
:9183 IB.TEST?,J/C.IQ ;
:9184
:9185 ;-----;
:9186 D_Q,Q_D,CLR.IB.SPEC,RETURN10 ;
:9187
:9188 ; ****
:9189 ; * Patch no. 047, PCS 04D3 trapped to WCS 116F *
:9190 ; ****
:9191
:9192 .LIST ;Re-enable full listing

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ZZ-ESOAA-124.0 : ARITH .MIC [600,1204] D 4  
: P1W124.MCR 600,1204] ARITH.MIC 14-Jan-82 14-Jan-82 Fiche 2 Frame D4 Sequence 248  
: ARITH .MIC [600,1204] MICRO2 1L(03) 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 247

:9193 .TOC "'ARITH.MIC'"  
:9194 .TOC "Revision 1.2"  
:9195 : P. R. Guilbault  
:9196

:9197 .NOBIN "  
:9198 .TOC " Revision History"

:9199  
:9200 : 01 Remove absolute jumps.  
:9201 : Change macro names that deal with condition codes.  
:9202 : 00 Delete MUL.MIC and put its code here.  
:9203 : Start of history  
:9204

:9205 .BIN  
:9206 .NOLIST :Disable listing of PCS code for quickie assemblies

E 4

:9207 .TOC " Integer arithmetic : Multiplication subroutine"  
 :9208  
 :9209 :THE MULTIPLICATION IS DONE 2 BITS PER CYCLE. THE MULTILICAND IS IN LB.  
 :9210 :THE 2 TIMES MULTPLICAND IS IN LC, AND THE MULTIPLIER IS IN D.  
 :9211 :SC SHOULD HAVE 3/7/15, FOR B/W/L MULTIPLICATIONS.  
 :9212 :THERE SHOULD BE 'ALU 0,D,D,RIGHT2,SI/ZERO,MUL?' IN THE CALLING STATE.  
 :9213 :DURING MULTIPLYING, THE PARTIAL PRODUCT IS IN D.  
 :9214 :WHEN DONE, THE PRODUCT IS IN Q AND D, WITH LSB'S IN D, AND SIGN EXTENDED IN Q.  
 :9215  
 :9216 :+VE MEANS LAST OPERATION IS POSITIVE, SUCH AS +2, OR +0.  
 :9217 : -VE MEANS LAST OPERATION IS NEGATIVE, SUCH AS -1, OR -0.  
 :9218 :+0 INDICATES TO DO DOUBLE RIGHT SHIFT BY 2 AND GO TO "+VE" COLUMNS FOR  
 :9219 :NEXT OPERATION. -2 INDICATES TO SUBTRACT 2 TIMES THE MULTPLICAND  
 :9220 :(LC HAS 2 TIMES MULTI'CAND, LB HAS MULTI'CAND) DO A DOUBLE RIGHT SHIFT  
 :9221 :BY 2, AND GO TO "-VE" COLUMNS OF THE TABLE.  
 :9222 :0XT, 1XT MEAN 0 EXTENDED, 1 EXTENDED WHEN SHIFTING, RESPECTIVELY.  
 :9223 :RETURN TO RETURN ADDR .OR. 2 WHEN DONE FOR POSITIVE PRODUCT. SET SC TO -16.  
 :9224 :RETURN TO RETURN ADDR .OR. 2 WHEN DONE FOR NEGATIVE PRODUCT. SET SC TO -16.  
 :9225  
 :9226 :

D<1:0>	MULT'CAND IS POSITIVE		MULT'CAND IS NEGATIVE	
	+VE	-VE	+VE	-VE
	MULPP	MULPM	MULMP	MULMM

  
 :9227 :-----  
 :9228 :  
 :9229 :  
 :9230 :  
 :9231 :  
 :9232 :  
 :9233 :  
 :9234 :  
 :9235 :  
 :9236 :  
 :9237 : (\*) THIS IS ONLY TRUE ONCE A NON-ZERO BIT OF THE MULTIPLIER HAS BEEN  
       ENCOUNTERED. UNTIL THEN THE OPERATION USED IS +0, 0XT  
       (I.E., RECOGNIZING THE FACT THAT A NEGATIVE 0 IS POSITIVE)

	:9238 ;	MULTIPLY LOOPS - EXPLANATION ON PREVIOUS PAGE	
	:9239		
	:9240 =000		
U 0350, 0200,003E,6F00,F800,4084,6002	:9241 MULPP: SC_K[.FFF0],MULP.DONE,RETURN2	:RETURN TO RETURN ADDR .OR. ?	
U 0351, 0200,003E,6F00,F800,4084,6002	:9242 SC_K[.FFF0],MULP.DONE,RETURN2	; FOR POS PRODUCT	
U 0352, 0200,003E,6F00,F800,4084,6002	:9243 SC_K[.FFF0],MULP.DONE,RETURN2	; (LAST EXTENDED BITS ARE 0S)	
U 0353, 0200,003E,6F00,F800,4084,6002	:9244 SC_K[.FFF0],MULP.DONE,RETURN2	; SET SC TO 16.	
U 0354, 0281,2C3C,0740,F800,0084,A350	:9245 MULPP.4: QD_QD.RIGHT2, MUL.OXT,J/MULPP	; +0, OXT	
U 0355, 028D,2C14,0740,F800,0084,A350	:9246 QD_(Q+LB)D.RIGHT2,MUL.OXT,J/MULPP	; +1, OXT	
U 0356, 0291,2C00,07C0,F800,0084,A3A0	:9247 QD_(Q-LC)D.RIGHT2,MUL.1XT,J/MULPM	; -2, 1XT	
U 0357, 028D,2C00,07C0,F800,0084,A3A0	:9248 QD_(Q-LB)D.RIGHT2,MUL.1XT,J/MULPM	; -1, 1XT	
	:9249		
U 03A0, 0200,003E,6F80,F800,4084,6002	:9250 MULPM: SC_K[.FFF0],MULM.DONE,RETURN2	:RETURN TO RETURN ADDR .OR. 2	
U 03A1, 0200,003E,6F80,F800,4084,6002	:9251 SC_K[.FFF0],MULM.DONE,RETURN2	; FOR NEG PRODUCT	
U 03A2, 0200,003E,6F80,F800,4084,6002	:9252 SC_K[.FFF0],MULM.DONE,RETURN2	; (LAST EXTENDED BITS ARE 1S)	
U 03A3, 0200,003E,6F80,F800,4084,6002	:9253 SC_K[.FFF0],MULM.DONE,RETURN2	; SET SC TO 16.	
U 03A4, 028D,2C14,0740,F800,0084,A350	:9254 QD_(Q+LB)D.RIGHT2,MUL.OXT,J/MULPP	; +1, OXT	
U 03A5, 0291,2C14,0740,F800,0084,A350	:9255 QD_(Q+LC)D.RIGHT2,MUL.OXT,J/MULPP	; +2, OXT	
U 03A6, 028D,2C00,07C0,F800,0084,A3A0	:9256 QD_(Q-LC)D.RIGHT2,MUL.1XT,J/MULPM	; -1, 1XT	
U 03A7, 0281,2C3C,07C0,F800,0084,A3A0	:9257 QD_QD.RIGHT2, MUL.1XT,J/MULPM	; -0, 1XT	
	:9258		
	:9259		
	:9260		
	:9261 =000		
U 0380, 0200,003E,6F80,F800,4084,6002	:9262 MULMP: SC_K[.FFF0],MULM.DONE,RETURN2	:RETURN TO RETURN ADDR .OR. 2	
U 0381, 0200,003E,6F80,F800,4084,6002	:9263 SC_K[.FFF0],MULM.DONE,RETURN2	; FOR NEG PRODUCT	
U 0382, 0200,003E,6F80,F800,4084,6002	:9264 SC_K[.FFF0],MULM.DONE,RETURN2	; (LAST EXTENDED BITS ARE 1S)	
U 0383, 0200,003E,6F80,F800,4084,6002	:9265 SC_K[.FFF0],MULM.DONE,RETURN2	; SET SC TO 16.	
U 0384, 0281,2C3C,07C0,F800,0084,A380	:9266 QD_QD.RIGHT2, MUL.1XT,J/MULMP	; +0, 1XT	
U 0385, 028D,2C14,07C0,F800,0084,A380	:9267 QD_(Q+LB)D.RIGHT2,MUL.1XT,J/MULMP	; +1, 1XT	
U 0386, 0291,2C00,0740,F800,0084,A3F0	:9268 QD_(Q-LC)D.RIGHT2,MUL.OXT,J/MULMM	; -2, OXT	
U 0387, 028D,2C00,0740,F800,0084,A3F0	:9269 QD_(Q-LB)D.RIGHT2,MUL.OXT,J/MULMM	; -1, OXT	
	:9270		
	:9271 =000		
U 03F0, 0200,003E,6F00,F800,4084,6002	:9272 MULMM: SC_K[.FFF0],MULP.DONE,RETURN2	:RETURN TO RETURN ADDR .OR. 2	
U 03F1, 0200,003E,6F00,F800,4084,6002	:9273 SC_K[.FFF0],MULP.DONE,RETURN2	; FOR POS PRODUCT	
U 03F2, 0200,003E,6F00,F800,4084,6002	:9274 SC_K[.FFF0],MULP.DONE,RETURN2	; (LAST EXTENDED BITS ARE 0S)	
U 03F3, 0200,003E,6F00,F800,4084,6002	:9275 SC_K[.FFF0],MULP.DONE,RETURN2	; SET SC TO 16.	
U 03F4, 028D,2C14,07C0,F800,0084,A380	:9276 QD_(Q+LB)D.RIGHT2,MUL.1XT,J/MULMP	; +1, 1XT	
U 03F5, 0291,2C14,07C0,F800,0084,A380	:9277 QD_(Q+LC)D.RIGHT2,MUL.1XT,J/MULMP	; +2, 1XT	
U 03F6, 028D,2C00,0740,F800,0084,A3F0	:9278 QD_(Q-LC)D.RIGHT2,MUL.OXT,J/MULMM	; -1, OXT	
U 03F7, 0281,2C3C,0740,F800,0084,A3F0	:9279 QD_QD.RIGHT2, MUL.OXT,J/MULMM	; -0, OXT	
	:9280		
	:9281		
	:9282 =100		
U 0294, 0281,2C3C,0740,F800,0084,A294	:9283 MULMZ: QD_QD.RIGHT2, MUL.OXT,J/MULMZ	:NEGATIVE MULTIPLIES START HERE	
U 0295, 028D,2C14,07C0,F800,0084,A380	:9284 QD_(Q+LB)D.RIGHT2,MUL.1XT,J/MULMP	; +0, OXT	
U 0296, 0291,2C00,0740,F800,0084,A3F0	:9285 QD_(Q-LC)D.RIGHT2,MUL.OXT,J/MULMM	; +1, 1XT	
U 0297, 028D,2C00,0740,F800,0084,A3F0	:9286 QD_(Q-LB)D.RIGHT2,MUL.OXT,J/MULMM	; -2, OXT	

ZZ-ESOAA-124.0 ; ARITH .MIC [600,1204]  
: P1W124.MCR 600,1204]  
: ARITH .MIC [600,1204]

MICR02 1L(03) Integer arithmetic 14-Jan-82  
Integer arithmetic : Divide subroutine

G 4

Integer arithmetic 14-Jan-82

15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124

Fiche 2 Frame G4

Sequence 251

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U 01C3, 0C41,003E,45C0,F800,4000,0008

U 01C7, 042D,0C00,06A8,F800,0084,A1C3

U 040E, 001F,0002,45C0,F800,4000,0008

U 01D3, 0C41,003C,01C0,F800,0000,040E

U 01D7, 042D,0C00,06A8,F800,0084,A1D3

:9287 .TOC " Integer arithmetic : Divide subroutine"

:9288 :DESCRIPTION:

:9290 : RESTORING DIVIDE SUBROUTINE

:9291 : ENTER AT DIVOX TO PRODUCE POSITIVE QUOTIENT,

:9292 : ENTER AT DIV1X TO PRODUCE NEGATIVE QUOTIENT.

:9293 :INPUTS:

:9294 : HIGH DIVIDEND IN D, LOW DIVIDEND IN Q

:9295 : DIVISOR IN LB, STEP COUNT IN SC.

:9300 : ALL NUMBERS CONSIDERED POSITIVE

:9301 :OUTPUTS:

:9302 : QUOTIENT (+ OR -) IN Q, REMAINDER IN D. SC = 0.

:9303 :RETURNS: ALWAYS AT 8

:9304 :=011

:9305 :DIV00: :011-----;

:9306 : K[.8000],Q,D.RIGHT,

:9307 : SI/ZERO,D,Q,

:9308 : INTRPT,STROBE,RETURN8

:9309 :;

:9310 :;

:9311 :;

:9312 :DIVOX: :111-----;

:9313 : DK/DIV,Q,Q.LEFT,

:9314 : SHF/LEFT,SI/DIV,

:9315 : SC SC-K[.1],ALU\_D-LB,

:9316 : MU[?],J/DIV00

:9317 : ;+/+

:9318 :DIV111: :-----;

:9319 : K[.8000],Q,0-Q,

:9320 : INTRPT,STROBE,RETURN8

:9321 :;

:9322 :DIV11: :011-----;

:9323 : Q,D.RIGHT,

:9324 : SI/ZERO,D,Q,J/DIV111

:9325 : ;-/+: -RMD, -QUOT

:9326 :DIV1X: :111-----;

:9327 : DK/DIV,Q,Q.LEFT,

:9328 : SHF/LEFT,SI/DIV,

:9329 : SC SC-K[.1],ALU\_D-LB,

:9330 : MU[?],J/DIV11

:9331 : ;-/+

ZZ-ESOAA-124.0 ; ARITH .MIC [600,1204] H 4  
 : PTWT24.MCR 600,1204] MICRO2 1L(03) Integer arithmetic 14-Jan-82 Fiche 2 Frame H4 Sequence 252  
 : ARITH .MIC [600,1204] Integer arithmetic 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 251

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;9331 .TOC " Integer arithmetic : MULB2, MULB3, MULW2, MULW3, MULL2, MULL3"
;9332
;9333 ;      MUL(B/W/L)2      MULR.RX, PROD.MX
;9334 ;      MUL(B/W/L)3      MULR.RX, MULD.RX, PROD.WX
;9335 ;INTEGER MUL'S. ENTER HERE FROM B-FORK
;9336 ;MUL B/W/L 2: * -- REG
;9337 ;THE OPERANDS ARE IN LA AND D REGISTERS.
;9338
;9339 22D: -----
;9340     D_LA, Q_D          ; NEED TO SIGN EXT M'IER
;9341
;9342     -----
;9343     D.D.SXT[INST.DEP], ; SIGN EXT M'IER
;9344     RC[ET1] ALU,        ; SAVE IN RC 1
;9345     SC_K[.FF]           ; SETUP TO GET CONSTANT 100 (HEX)
;9346
;9347 =01*0 :00----- (IRO = 0)
;9348     Q.Q.SXT[INST.DEP]. ; SIGN EXTEND MUL'CAND
;9349     IB[ET0] D,          ; SAVE MUL'IER
;9350     SC SC+T,            ; SC GETS 100 (HEX)
;9351     CAEL,J/MUL.S       ;
;9352
;9353     :01----- POS
;9354     ALU Q, SET.CC(INST). ; SET PSL<V> IF OVERFLOW
;9355     J/MUL.0
;9356
;9357 MUL.0: :10----- RETURN HERE FOR PROD = 0
;9358     R(PRN) D,           ; STORE RESULT 0
;9359     DT/INST.DEP,         ; WRITE B/W/L TO R
;9360     CLR.IB.OPC,PC_PC+1. ; UPDATE IB, PC
;9361     J/IRD               ; GOTO NEXT INSTR
;9362
;9363     :11----- NEG
;9364     ALU_Q+K[.1],          ; SET PSL<V> IF OVERFLOW
;9365     SET.CC(INST),
;9366     J/MUL.0
;9367 =:END
  
```

	:9368 : INTEGER MUL'S. ENTER HERE FROM C-FORK	
	:9369 :MUL B/W/L 2: * -- NOT REG, * -- * -- *	
	:9370 :THE OPERANDS ARE IN D AND Q REGISTERS.	
	:9371	
	:9372 381:	
	:9373 MUL: -----	
U 0381, 0802,C03C,4980,F988,0084,6506	:9374 D.D.SXT[INST.DEP]. : SIGN EXT M'IER	
	:9375 RC[T1] ALU. : SAVE IN RC 1	
	:9376 SC_K[.FF] : SETUP TO GET CONSTANT 100 (HEX)	
	:9377	
U 0506, 0002,E03D,C1C0,3C00,0080,C430	:9378 =0110 :00-----	
	:9379 Q.Q.SXT[INST.DEP]. : SIGN EXTEND MUL'CAND	
	:9380 ID[T0] D, : SAVE MUL'IER	
	:9381 SC_SC+T, CALL, J/MUL.S : SC GETS 100 (HEX). CALL MUL SUBR	
U 0507, F001,E03F,01F0,F847,0070,0300	:9382 :01-----	
	:9383 ALU_Q.SET.CC(INST). : POS	
	:9384 WRITE.DEST,J/WRD : SET PSL<V> IF OVERFLOW	
	:9385	WRITE RESULT
U 050E, F818,C03B,19FC,F847,0070,0300	:9386 :10-----	RETURN HERE FOR PROD = 0
	:9387 D_K[ZERO], : PROD IS 0	
	:9388 SET.CC(INST), : SFT COND CODES	
	:9389 WRITE.DEST,J/WRD : WRITE RESULT	
U 050F, F019,E017,05F0,F847,0070,0300	:9390 :11-----	NEG
	:9391 ALU_Q+K[.1], : SET PSL<V> IF OVERFLOW	
	:9392 SET.CC(INST), : WRITE RESULT	
	:9393 WRITE.DEST,J/WRD	
	:9394	
	:9395	
	:9396 =:END	

ZZ-ESOAA-124.0 ; ARITH .MIC [600,1204] Integer arithmetic 14-Jan-82 Fiche 2 Frame J4 Sequence 254  
 : P1W124.MCR 600,1204] MICRO2 1L(C3) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 253  
 ; ARITH .MIC [600,1204] Integer arithmetic : MULB2, MULB3, MULW2, MULW3, MULL2, MULL3

J 4

:9397 : COMMON SIGNED MULTIPLY SUBROUTINE FOR BYTE, WORD, LONGWORD  
 :9398 :  
 :9399 : INPUTS:  
 :9400 : SIGN-EXTENDED MULTIPLIER IN D, COPIES IN RC[T1] AND ID[T0].  
 :9401 : MULTIPLICAND (ALSO SIGN EXTENDED) IN Q  
 :9402 : SC = 100(HEX)  
 :9403 : INSTRUCTION DECODE ROMS DETERMINE DATA TYPE  
 :9404 :  
 :9405 : OUTPUTS:  
 :9406 : D = LOW 32 BITS OF PRODUCT  
 :9407 : Q = BITS OF PRODUCT WHICH DON'T FIT IN RESULT  
 :9408 :  
 :9409 : RETURNS:  
 :9410 : RETURNS AT 1 IF PRODUCT > 0  
 :9411 : RETURNS AT 8 IF PRODUCT = 0  
 :9412 : RETURNS AT 9 IF PRODUCT < 0  
 :9413 :  
 :9414 : TEMPORARIES:  
 :9415 : R15 USED TO SAVE MULTIPLICAND  
 :9416 : STATE USED TO HOLD DATA-TYPE DEPENDENT SHIFT COUNTS  
 :9417 : FE DITTO  
 :9418 : LA,LB,LC USED IN MULTIPLY LOOP  
 :9419 :  
 :9420 :  
 :9421 : MUL.S: -----:  
 :9422 : R[R15] Q, D Q, : SAVE M'CAND  
 :9423 : SC SC+R[SC], : SC NOW CONTAINS 200  
 :9424 : D.NE.0? : MUL'IER IS 0?  
 :9425 :  
 :9426 : =101 :0-----:  
 :9427 : D K[ZERO],N&Z\_ALU.V&C\_0,: PROD IS 0 SINCE MUL'IER IS 0  
 :9428 : RETURN8 : WRITE RESULT 0  
 :9429 :  
 :9430 : :1-----:  
 :9431 : Q\_K[SC].CTX, : SET SHF COUNT FOR B,W,L  
 :9432 : LAB\_R[R15] : LATCH MUL'CAND  
 :9433 : =:END :  
 :9434 : -----:  
 :9435 : SC\_Q(EXP), STATE\_Q(EXP),: SC GETS COUNT (4,8,16) FOR B,W,L VIA EBMX  
 :9436 : FE\_Q(EXP), Q D, BK/SHF, : SAVE CT TO REMEMBER B,W,L  
 :9437 : RC[T0]\_LB.LEFT,SI/ZERO : RC 0 GETS 2 TIMES M'CAND  
 :9438 :  
 :9439 : =0\*:0-----:  
 :9440 : D RC[T1],Q,0, : D GETS M'IER  
 :9441 : STATE\_STATE+FE, : STATE HAS # BITS (8,16,32) FOR B,W,L  
 :9442 : CALL,SIGNS?, J/MUL.6 : POS OR NEG MUL'CAND?  
 :9443 :

U 0430, 0C01,2D3C,1D80,FAF8,0084,8135  
 U 0135, 0818,003A,1980,F800,0050,0008  
 U 0137, 0078,C038,1DC0,FA78,0000,043A  
 U 043A, 082D,2038,01E0,F980,1588,6068  
 U 0068, 0810,0D39,01F8,F908,1400,82A1

ZZ-ESOAA-124.0 ; ARITH .MIC [600,1204]  
: P1W124.MCR 600,1204]  
: ARITH .MIC [600,1204]

K 4  
MICR02 1L(03) Integer arithmetic 14-Jan-82  
14-Jan-82 15:30:16

VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124

Fiche 2 Frame K4

Sequence 255

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Integer arithmetic : MULB2, MULB3, MULW2, MULW3, MULL2, MULL3

U 006A, 0001,003C,758C,F800,1494,A464

:9444 :-----  
:9445 ALU\_D, CLK,UBCC,  
:9446 STATE STATE-K[.20],  
:9447 SC\_EAU  
=:END :-----  
:9449 D\_DAL.SC :-----  
:9450 :-----  
:9451 :-----  
:9452 :-----  
:9453 ALU\_D, N8Z ALU.V&C\_0,  
:9454 DT/INST.DEP  
:9455 ALU.N?, RETURN1 :-----  
:9456 :-----  
:9457 =001 :00-----  
:9458 MUL.6: :00-----  
:9459 D\_K[ZERO], Q\_0,  
:9460 N8Z ALU.V&C\_0,  
:9461 RETURN2 :-----  
:9462 :01-----  
:9463 SC\_SC-K[.1],  
:9464 LC\_RC[T0], ALU\_0(A),  
:9465 D\_D.RIGHT2, SI7ZERO,  
:9466 MUL?, J/MULPP :-----  
:9467 :10-----  
:9468 Q\_0-D,D\_0,  
:9469 J7MUL.8 :-----  
:9470 :11-----  
:9471 SC\_SC-K[.1],  
:9472 LC\_RC[T0], ALU\_0(A),  
:9473 D\_D.RIGHT2, SI7ZERO,  
:9474 MUL?, J/MULMZ :-----  
:9475 :-----  
:9476 :-----  
:9477 :-----  
:9478 =:END :-----  
:9479 :-----  
:9480 :-----  
:9481 ALU\_Q,Q\_ALU.RIGHT,  
:9482 D\_D.RIGHT,SI/ASHR,  
:9483 RETURN2 :-----

D31 HAS HI BIT OF PROD - ALU.N=SIGN  
STATE GETS -24, -16, 0 FOR B,W,L  
MORE IMPORTANTLY, SO DOES SC

ALIGN PRODUCT FOR BYTE, WORD, LONG INSTR

SET COND CODES, N & Z  
DATA TYPE SET FOR B/W/L  
IS PROD POS OR NEG?

M'CAND IS 0  
PROD IS 0 SINCE MUL'CAND IS 0  
SET COND CODES  
WRITE RESULT 0

SC HAS LOOP COUNT (3,7,15) FOR B,W,L  
LATCH 2 TIMES MUL'CAND, SETUP ALU[1:0]  
SHIFT MUL'IER BY 2 BITS  
GOTO MULT ROUTINE

M'CAND IS MOST NEG NUMBER FOR MULL  
NEG M'IER

SC HAS LOOP COUNT (3,7,15) FOR B,W,L  
LATCH 2 TIMES MUL'CAND, SETUP ALU[1:0]  
SHIFT MUL'IER BY 2 BITS  
GOTO MULT ROUTINE AT INITIAL NEG ENTRY PT

ARITH SHF RIGHT <Q,D>

U 046D, 0001,DB3E,0180,F800,0050,0001

U 02A1, 0818,003A,19F8,F800,0050,0002

U 02A3, 0203,0C3C,0580,F900,0084,A350

U 02A5, 0F1F,2000,01C0,F800,0000,0475

U 02A7, 0203,0C3C,0580,F900,0084,A294

U 0475, 0641,203E,00C0,F800,0000,0002

ZZ-ESOAA-124.0 ; ARITH .MIC [600,1204] Integer arithmetic 14-Jan-82 Fiche 2 Frame L4 Sequence 256  
 : PTWT24.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 255  
 : ARITH .MIC [600,1204] Integer arithmetic : EMUL

L 4

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:9484 .TOC   "      Integer arithmetic : EMUL"
:9485
:9486 :     EMUL    7A    MULR.RL, MULD.RL, ADD.RL, PROD.WQ
:9487 :EMUL: EXTEND INTEGER MULTIPLICATION.
:9488 :THE MULT'CAND IS IN D, AND THE MULT'IER IS IN Q.
:9489
:9490 :     DOES NOT USE THE SAME ROUTINE USED BY NORMAL INTEGER MULTIPLIES.
:9491 :     BUT INSTEAD CALLS THE LOW LEVEL MUL ROUTINE DIRECTLY.
:9492 :     THE ADDEND IS ADDED AS A SEPARATE STEP INSTEAD OF 'FOR FREE'
:9493 :     DURING THE MULTIPLY LOOP BECAUSE OF OVERFLOW PROBLEMS IN THE LOOP.
:9494
:9495 389:
:9496 EMUL: -----
:9497 R[R15]_D,          : R15 GETS MULT'CAND
:9498 Q_D, D_Q,          : SWAP D, AND Q
:9499 D.NE.0?            : MULT'CAND .NE. 0?
:9500
:9501 =101 :0-----: NO: MULT'CAND = 0, THEREFORE PRODUCT = 0
:9502      D_0, ID[T0]_D, : SET PROD TO 0
:9503      J7EMUL.2       : GOTO ADD ADDEND
:9504
:9505 :1-----: YES: MULT'CAND NE 0, CHECK IF MULT'IER = 0
:9506 R[C[T0]]_Q.LEFT, SI/ZERO.: RCO GETS 2 TIMES MULT'CAND
:9507 SIGNS?             : MULT'IER .NE. 0?
:9508 =:END
:9509
:9510 =001 :00-----: NO: MULT'IER = 0, THEREFORE PROD = 0
:9511      Q_0,           : SET PROD TO 0
:9512      J7EMUL.2       : GOTO ADD ADDEND
:9513
:9514 :01-----: YES: PROD .NE. 0, M'CAND POS
:9515 LAB_R[R15],         : LB GETS MULT'CAND
:9516 Q_0, SC_K[F].      : PARTIAL PROD RESET TO 0, LOOP COUNT SET FOR 16.
:9517 J7EMUL.T            : GOTO POS ROUTINE
:9518
:9519 :10-----: NO: MULT'IER = 0, THEREFORE PROD = 0
:9520      Q_0,           : SET PROD TO 0
:9521      J7EMUL.2       : GOTO ADD ADDEND
:9522
:9523 :11-----: YES: PROD .NE. 0, M'CAND NEG
:9524 LAB_R[R15],         : LB GETS MULT'CAND
:9525 Q_0, SC_K[F]        : PARTIAL PROD RESET TO 0, LOOP COUNT SET FOR 16.
:9526
:9527 : ****
:9528 : * Patch no. 029, PCS 02B7 trapped to WCS 1161 *
:9529 : ****
:9530 =:END
:9531
:9532 =0***0*
:9533 AR.PA.29:
:9534 :0-----:
:9535      LC_RC[T0],      : LATCH 2 TIMES M'CAND IN LC
:9536      ALU_0(A),        : SET ALU[1:0] TO 0
:9537      D.D.RIGHT2, SI/ZERO, : READY FOR MUL ROUTINE
:9538      CALL, MUL?: J/MULMZ : GOTO NEG M'CAND MULTIPLICATION ROUTINE
  
```

U 0389, 0001,0D3C,01EC,FAF8,0000,01A5
 U 01A5, 0F00,003C,C180,3C00,0000,02A2
 U 01A7, 0021,2D3C,0180,F980,0000,02B1
 U 02B1, 0000,003C,01F8,F800,0000,02A2
 U 02B3, 0000,003C,61F8,FA78,0084,62A0
 U 02B5, 0000,003C,01F8,F800,0000,02A2
 U 02B7, 0000,003C,61F8,FA78,0084,61C0
 U 01C0, 0203,0C3D,0180,F900,0000,0294

ZZ-ESOAA-124.0 ; ARITH .MIC [600,1204] Integer arithmetic 14-Jan-82 M 4  
; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Sequence 257  
; ARITH .MIC [600,1204] Integer arithmetic : EMUL Page 256

;9539  
;9540 =0\*\*1\* ;1-----  
;9541 R[R15].Q,  
;9542 CALL, INTERRUP.TREQ?,  
;9543 J/SPEC  
;9544  
;9545 =1\*\*1\* ;1\*\*1\*-----  
;9546 D,D+Q, CLK,UBCC,  
;9547 LAB,R[R15],  
;9548 D31?, J/EMUL.3  
;9549 =:END  
U 01C2, 0001,2E3D,0180,FAF8,0000,037E  
U 01D2, 081D,0D14,0180,FA78,0010,0156

Fiche 2 Frame M4

Sequence 257

Page 256

SAVE PROD <H>

GET ADDEND

ADD ADDEND, CLOCK IN CARRY

LATCH PROD <H>

IS ADDEND NEG?

U 02A0, 0203,0C3D,0180,F900,0000,0357

:9550 =0\*\*0\*  
 :9551 EMUL.1: -----  
 :9552 LC RC[TO],  
 :9553 ALU\_0(A),  
 :9554 D.D.RIGHT2, SI/ZERO,  
 :9555 CALL, MUL?, J/MULPP ; LATCH 2 TIMES M'CAND IN LC  
 :9556 =0\*\*1\* ; SET ALU[1:0] TO 0  
 :9557 EMUL.2: ----- ; READY FOR MULT ROUTINE  
 :9558 R[R15] Q,  
 :9559 CALL, INTERRUPT.REQ?,  
 :9560 J/SPEC ; GOTO POS M'CAND MULTIPLICATION ROUTINE  
 :9561

U 02A2, 0001,2E3D,0180,FAF8,0000,037E

:9562 =0\*\*1\* :1\*\*1\*-----  
 :9563 D.D+Q, CLK.USCC,  
 :9564 LAB\_R[R15],  
 :9565 D31? ; ADD ADDEND, CLOCK IN CARRY  
 :9566 =;END ; LATCH PROD <H>  
 :9567 ; IS ADDEND NEG?  
 :9568 =110

U 02B2, 081D,0D14,0180,FA78,0010,0156

:9569 EMUL.3: :0-----  
 :9570 ALU\_D.SET.CC(INST),  
 :9571 C31?, J/EMUL.4 ; SET COND CODES PART 1  
 :9572

U 0156, 0001,C33C,0180,F800,0070,0250

:9573 :1-----  
 :9574 ALU\_D.SET.CC(INST),  
 :9575 C31? ; SET COND CODES PART 1  
 :9576 =;END ; CARRY TO PROD <H>?

U 0157, 0001,C33C,0180,F800,0070,00E8

:9578 =0\* :0-----  
 :9579 Q\_LA-K[.1],RC[T1]\_ALU,  
 :9580 J7EMUL.6 ; GET PROD <H>  
 :9581

U 00E8, 0018,0000,05C0,F988,0000,0492

:9582 :1-----  
 :9583 RC[T1] LA,  
 :9584 N\_AMX.Z\_TST,  
 :9585 J7WRDST ; PROD <H>  
 :9586 =;END ; SET COND CODES PART 2  
 :9587

U JOEA, 0000,003C,0180,F988,0030,0603

:9588 EMUL.6: -----  
 :9589 ALU\_Q,N\_AMX.Z\_TST,  
 :9590 WRITE.DEST, J7WRD ; SET COND CODES PART 2  
 :9591

U 0492, F001,203F,01F0,F847,0030,0300

:9592 =0\* :0-----  
 :9593 EMUL.4: RC[T1] LA,  
 :9594 N\_AMX.Z\_TST,  
 :9595 J7WRDST ; PROD <H>  
 :9596

U 0250, 0000,003C,0180,F988,0030,0603

:9597 :1-----  
 :9598 Q\_LA+K[.1],RC[T1]\_ALU,  
 :9599 J7EMUL.6 ; SET COND CODES PART 2  
 :9600 =;END ; GOTO WRITE DEST

U 0252, 0018,0014,05C0,F988,0000,0492

:9601 :1-----  
 :9602 Q\_LA+K[.1],RC[T1]\_ALU,  
 :9603 J7EMUL.6 ; RC1 GETS PROD <H>  
 :9604 =;END ; GOTO SET COND CODES

B 5

ZZ-ESOAA-124.0 ; ARITH .MIC [600,1204] Integer arithmetic 14-Jan-82 Fiche 2 Frame B5 Sequence 259  
 : P1W124.MCR 600,1204] MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 258  
 ; ARITH .MIC [600,1204] Integer arithmetic : DIVB2, DIVB3, DIVW2, DIVW3, DIVL2, DIVL3

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;9601 .TOC " Integer arithmetic : DIVB2, DIVB3, DIVW2, DIVW3, DIVL2, DIVL3"
;9602
;9603 ; DIV(B/W/L)2 DIVR.RX, QUO.MX
;9604 ; DIV(B/W/L)3 DIVR.RX, DIVD.RX, QUO.WX
;9605 ;INTERGER DIV. ENTER AT B.FORK WITH D'END IN LA AND D'SOR IN D.
;9606
;9607 22C: -----
;9608   Q_D, D_LA           ; D GE IS D'END, Q GETS D'SOR, SIGN EXT LATTER
;9609
;9610
;9611   D_Q.SXT[INST.DEP], ; SIGN EXT D'SOR
;9612   Q_D                 ; Q GETS D'END
;9613   STATE_K[ZERO]       ; CLEAR FLAG (USED FOR NEG QUOT)
;9614
;9615   -----
;9616   R[R15]_D             ; SAVE D'SOR
;9617
;9618 =0***0 :00
;9619   D_Q.SXT[INST.DEP], Q_0, ; SXT EXT D'END, Q=0 TO HACK CONSTRAINT @DIV.2
;9620   LAB R[R15]             ; LATCH D'SOR
;9621   CALL[SIGNS?],J/DIV.S  ; D.NE.0? D31?
;9622
;9623   :01-----; RETURN HERE FOR DIV BY 0
;9624   J/DIV.Z0
;9625
;9626   :10-----; RETURN HERE WITH D HAS QUOT
;9627   Q_D.SXT[INST.DEP], D_0, ; Q GETS QUOT, D=0 FOR CONSTRAINT HACK & NEGATE
;9628   STATE0?               ; HAVE TO NEGATE QUOTIENT?
;9629
;9630 =;END :0-----; NO: +/- OR -/-
;9631   R(PRN) Q, N&Z_ALU.V&C_0, ; SET COND CODES
;9632   DT/INST.DEP,             ; WRITE ONLY B/W/L IN R
;9633   Q31?,J/DIV.OV           ; OVERFLOW?
;9634
;9635   :1-----; YES: +/- OR -/+
;9636   R(PRN) ALU,ALU_D-Q,    ; NEGATE QUOTIENT
;9637   N&Z_ALU.V&C_0,          ; SET COND CODES
;9638   DT/INST.DEP,             ; WRITE ONLY B/W/L IN R
;9639   CLR.IB.OPC,PC_PC+1,     ; UPDATE IB, PC
;9640   J/IRD                  ; GOTO NEXT INST
;9641
;9642 =;END :0-----; NO OVERFLOW
;9643
;9644 =0*0 DIV.OV: :0-----; DIV.OV: CLR.IB.OPC, PC_PC+1,
;9645   J/IRD                  ; J/IRD
;9646
;9647 =1*0 :1-----; Q_ID[CES], CALL[INOVFL]
;9648   Q_ID[CES], CALL[INOVFL]; GO SET V AND TRAP CODE
;9649
;9650
;9651
;9652   :-----; RETURN FROM INOVFL HERE
;9653   CLR.IB.OPC,PC_PC+1,     ; UPDATE IB, PC
;9654   J/IRD                  ; NEXT INST
;9655

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ZZ-ES0AA-124.0 ; ARITH .MIC [600,1204] Integer arithmetic 14-Jan-82 C 5  
; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Sequence 260  
; ARITH .MIC [600,1204] Integer arithmetic : DIVB2, DIVB3, DIVW2, DIVW3, DIVL2, DIVL3 Page 259

U 0280, 0000,003D,31F0,2C00,0000,0DFD :9656 =0  
U 0281, C000,003C,0180,F804,4000,0062 :9657 DIV.Z0: ;0-----;  
:9658 Q\_ID[CES], : GET CES  
:9659 CALL,J/INDIVO : CALL SETUP CES  
:9660  
:9661 ;1-----;  
:9662 CLR,IB,OPC,PC\_PC+1, : UPDATE IB, PC  
:9663 J/IRD : NEXT INST  
:9664 =;END

D 5

ZZ-ESOAA-124.0 ; ARITH .MIC [600,1204] Integer arithmetic 14-Jan-82 Fiche 2 Frame D5 Sequence 261  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 260  
 : ARITH .MIC [600,1204] Integer arithmetic : DIVB2, DIVB3, DIVW2, DIVW3, DIVL2, DIVL3

U 0380, 081A,E014,19E0,F800,1414,64EA	:9665 :INTERGER DIV, ENTER AT C.FORK WITH D'END IN D AND D'SOR IN Q.
U 04EA, 0001,003C,0180,FAF8,0000,0270	:9666 :580:
	:9667 DIV: -----
	:9668 ALU_Q.SXT[INST.DEP]+K[ZERO], ; SIGN EXT D'SOR
	:9669 D_A[U,CLK,UBCC,Q_D, ; Q GETS D'END
	:9670 STATE_K[ZERO] ; CLEAR FLAG (USED FOR NEG QUOT)
	:9671
	:9672 -----
	:9673 R[R15]_D ; SAVE D'SOR
	:9674
	:9675 =0***0 :00-----
	:9676 D_Q.SXT[INST.DEP], Q_0, ; SXT EXT D'END, Q=0 FOR CONSTRAINT HACK @DIV.2
	:9677 LAB_R[R15], ; LATCH D'SOR
	:9678 CALL,SIGNS?,J/DIV.S ; D.NE.0? D31?
	:9679 :01-----
	:9680 D_Q.SXT[INST.DEP], ; RETURN HERE FOR DIV BY 0
	:9681 IR0?, J/DIV.Z ; SXT EXT D'END
	:9682 IF 2-OPR INST, DO NOT CHANGE QUOT OPR
	:9683 :10-----
	:9684 Q_D.SXT[INST.DEP], D_0, ; RETURN HERE WITH D HAS QUOT
	:9685 STATE3-0? ; Q GETS QUOT, D=0 FOR CONSTRAINT HACK
	:9686 HAVE TO NEGATE QUOT?
	:9687 =;END
	:9688
	:9689 =**10 :0-----
	:9690 ALU_Q,D_ALU,DT/INST.DEP, ; MOVE QUOT TO D
	:9691 NZ_ALU.V&C_0, ; SET COND CODES
	:9692 Q31?, J/DIV.OV3 ; OVERFLOW?
	:9693 :1-----
	:9694 D_D-Q, NZ_ALU.V&C_0, ; YES: +/- OR -/+
	:9695 DT/INST.DEP, ; SET COND CODES BY NEG QUOT
	:9696 WRITE.DEST ; DATA TYPE SET FOR B/W/L
	:9697
	:9698 =;END
	:9699
	:9700 =0*0 :0-----
	:9701 DIV.OV3: WRITE.DEST ; NO OVERFLOW
	:9702 JUST WRITE & LEAVE
	:9703 =1*0 :1-----
	:9704 Q_ID[CES], CALL[INOVFL] ; OVERFLOW - MAX NEG # / -1
	:9705 SET TRAP CODE AND V BIT
	:9706 :-----
	:9707 WRITE.DEST ; INOVFL RETURNS HERE
	:9708 =;END
	:9709
	:9710 =*100 :00-----
	:9711 DIV.Z: J/DIV.Z0 ; (SINCE DIVISOR=0, ALU.N=0)
	:9712 2-OPR INST, DO NOT CHANGE QUOT OPR
	:9713
	:9714 =*110 :10-----
	:9715 Q_ID[CES], CALL[INDIVO] ; 3-OPR INST, QUOT OPR GETS D'END
	:9716 GET CES, GO SET TRAP CODE & V BIT
	:9717
	:9718 =;END
	:9719 :11-----
	WRITE.DEST ; WRITE QUOT

E 5

ZZ-ESOAA-124.0 ; ARITH .MIC [600,1204] Integer arithmetic 14-Jan-82 Fiche 2 Frame E5 Sequence 262  
; P1W124.MCR 600,1204] MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 261  
; ARITH .MIC [600,1204] Integer arithmetic : DIVB2, DIVB3, DIVW2, DIVW3, DIVL2, DIVL3

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;9720 ;SUBROUTINE TO DO BYTE, WORD OR LONGWORD DIVISION.
;9721 ;USES RESTORING DIVIDE SUBROUTINE DIVOX.
;9722 ;ENTER AT DIV.S WITH BEN/SIGNS TESTING DIVISOR-WHICH WAS IN D TILL CALLING STATE
;9723
;9724 ;INPUTS: DIVISOR (SIGN EXTENDED TO LONGWORD) IN R15 WITH A COPY IN LA&LB.
;9725 ; DIVIDEND (ALSO SIGN EXTENDED) IN D
;9726 ; Q = STATE = 0.
;9727
;9728 ;OUTPUTS: Q = ABSOLUTE VALUE OF QUOTIENT
;9729 ; D = ABSOLUTE VALUE OF REMAINDER
;9730 ; STATE<0> = DESIRED QUOTIENT SIGN(1 MEANS QUOTIENT IN Q NEEDS NEGATING)
;9731
;9732 ;RETURNS: RETURNS AT 1 IF DIVISOR = 0
;9733 ; RETURNS AT 8 OTHERWISE
;9734
;9735 ;TEMPORARIES: SC USED FOR STEP COUNTER
;9736 ; R15,LA,LB DESTROYED
;9737
;9738 =100
;9739 DIV.S: ;00-----; D'SOR IS 0
;9740 ; ALU_D, N&Z ALU.VBC_0, ; SET COND CODES N & Z
;9741 ; DT/INST.DEP, ; DATA TYPE SET FOR B/W/L
;9742 ; RETURN1 ; D'SOR IS 0
;9743
;9744 ; ****
;9745 ; * Patch no. 034, PCS 0374 trapped to WCS 1166 *
;9746 ; ****
;9747
;9748 =110
;9749 DIV.0: ;10-----; D'SOR ,NE, 0, AND IS POS
;9750 ; Q_K[.8].CTX, ; SET LOOP CT OF 8,16,32 FOR B,W,L
;9751 ; LAB_R[R15], ; LATCH ABS(D'SOR)
;9752 ; D31?,J/DIV.2 ; IS D'END POS OR NEG?
;9753
;9754 ;11-----; D'SOR ,NE, 0, AND IS NEG
;9755 ; R[R15] ^-LB, ; R15 GETS ABS(D'SOR)
;9756 ; STATE_STATE+1,J/DIV.0 ; EXCLUSIVE OR STATE[00] AS FLAG FOR NEGATE QUOT
;9757
;9758 =;END
;9759 =*10
;9760 DIV.2: ;0-----; TO ALIGN D'END, LEFT JUSTIFIED IN Q
;9761 ; ALU_0-Q_SC_ALU, ; SC GETS -8,-16.,-32. FOR B,W,L
;9762 ; Q_D_D_0, ; Q GETS D'END
;9763 ; J7DIV.3 ; GOTO ALIGN D'END
;9764
;9765 ;1-----; D GETS ABS(D'END) FOR NEG D'END
;9766 ; D_0-D,
;9767 ; STATE_STATE+1,J/DIV.2 ; EXCLUSIVE OR STATE[00] AS FLAG FOR NEGATE QUOT
;9768
;9769 =;END
;9770 DIV.3: ;-----;
;9771 ; D_DAL.SC,
;9772 ; SC_0-K[SC] ; D GETS D'END LEFT JUSTIFIED
;9773 ; SC GETS LOOP CT 8,16.,32. FOR B,W,L
;9774
;9775 ;-----;
;9776 ; Q_D_D_0,
;9777 ; J7DIVOX ; Q GETS D'END
;9778 ; GOTO DIVIDE ROUTINE
;9779

```

U 0374, 0001,C03E,0180,F800,0050,0001

U 0376, C078,CD38,01C0,FA78,0000,02C2

U 0377, 000F,0000,0180,FAF8,1400,C376

U 02C2, 0F1F,0000,01E0,F800,0082,04EE

U 02C3, 081F,2000,0180,F800,1400,C2C2

U 04EE, 0D1B,0000,1D80,F800,0082,04F1

U 04F1, 0F00,003C,01E0,F800,0000,01C7

F 5

ZZ-ESOAA-124.0 : ARITH .MIC [600,1204] Integer arithmetic 14-Jan-82 Fiche 2 Frame F5 Sequence 263  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 262  
 ; ARITH .MIC [600,1204] Integer arithmetic : EDIV

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;9774 .TOC   " Integer arithmetic : EDIV"
;9775
;9776 : EDIV (7B) DIVR.RL, DIVD.RQ, QUO.WL, REM.WL
;9777 : INTERGER EXTENDED DIVIDE. EDIV, WITH D'END IN <D, RC1> AND D'SOR IN Q.
;9778 388:
;9779 EDIV: -----
;9780     R[R15]_Q,          : R15 GETS D'SOR
;9781     D_Q, Q_D,          : D GETS D'SOR. Q GETS D'END <H>
;9782     ID[T0]_D           : SAVE D'END<H> IN CASE WE OVERFLOW
;9783
;9784
;9785     SC_K[.20].ALU,      : SET LOOP COUNT
;9786     STATE_O(A).LC_RC[T1], : LATCH D'END <L>
;9787     D_Q, Q_D,          : D GETS D'END <H>, Q GETS D'SOR
;9788     SIGNS?              : D'SOR = 0? POS OR NEG?
;9789
;9790 =0100 :00-----: D'SOR = 0
;9791     D_RC[T1],          : D GETS DIVIDEND<31:0>
;9792     NZ_ALU.VBC_0, J/EDIV.Z : SET CCL 5 ON D'END <L>
;9793
;9794 EDIV.1: :10-----: D'SOR IS POS
;9795     LAB_R[R15],          : LATCH D'SOR IN LB
;9796     ALU_LC, CLK.UBCC,    : SET ALU.Z IF DIVIDEND<L>=0
;9797     CALL, D31?, J/EDIV.6 : D'END POS OR NEG?
;9798
;9799 :11-----: D'SOR IS NEG
;9800     R[R15]_0-Q,          : R15 GETS ABS(D'SOR)
;9801     STATE_STATE+1, J/EDIV.1 : EXCL OR STATE[00] AS FLAG FOR NEGATE QUOT
;9802
;9803 =1110 :-----: RETURN HERE WITH QUOT IN D, REM IN Q
;9804     ALU_0+D, CLK.UBCC,    : SHOULD QUOTIENT BE POS OR NEG?
;9805     STATE0?              :
;9806
;9807 =:END :0-----: QUOT IS POS
;9808     ALU_D, NZ_ALU.VBC_0,  : SET CONDITION CODES ON QUOTIENT
;9809     ALU.N?, J/EDIV.9     : CHECK FOR OVERFLOW AND GO STORE
;9810
;9811 :1-----: QUOT IS NEG
;9812     ALU_D-K[.1],CLK.UBCC, Z?: SET UP OVFL0 TEST & CHECK IF 0
;9813
;9814 :*****: Patch no. 011, PCS 0413 trapped to WCS 1148 *
;9815 :*****:
;9816 :*****:
;9817 =:END :0-----: QUOT < 0
;9818     D_0-D, NZ_ALU.VBC_0,  : NEGATE QUOTIENT
;9819     ALU.N?, J/EDIV.9     : GO CHECK OVERFLOW (POS NUM > 2**31)
;9820
;9821 :1-----: QUOT = 0
;9822     ID[T0]_D, D_Q, SC_O(A), : QUO = D, REM = Q,
;9823     ALU_O(A), NZ_ALU.VBC_0, : SET COND CODES FOR A 0 RESULT
;9824     INTRPT_STROBE,        : USE EMODF CODE TO STORE RESULTS
;9825     STATE_O(A), J/EMODF.11 : SINCE A PAIR OF LWORDS IS A PAIR OF LWORDS
;9826

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U 0320, 0000,003D,31F0,2C00,0000,0DFC	:9827 =0	
	:9828 EDIV.2: ;0-----	OVERFLOW COMES HERE
	:9829 Q_ID[CES],	GET CES
	:9830 CALL,J/INOVFL	CALL SETUP CES
	:9831	
	:9832 :1-----	
	:9833 ID[T0]_D, D_0, SC_0(A),	QUO = D'END<L>, REM = 0,
	:9834 INTRPT_STROBE,	USE EMODF CODE TO STORE RESULTS
	:9835 STATE_0(A), J/EMODF.11	SINCE A PAIR OF LONGWORDS IS A PAIR OF LONGWORDS
	=;END	
	:9837 EDIV.3: -----	
	:9838 Q_RC[T1],Q31?	Q GETS D'END <L>, OVERFLOW?
	:9839	
	:9840 =01* ;0-----	OK (D KNOWN +)
	:9841 J/DIVOX	CALL DIV SUBRT
	:9842 :1-----	
	:9843 D_RC[T1],	OVERFLOW
	:9844 NZ_ALU.V&C_0, J/EDIV.2	Q GETS D'END <L>
	=;END	SET CCL 5 ON D'END <L>
	:9845 :1-----	
	:9846 D'_ALU.LA-D-1, Q_ALU,	D'END POS
	:9847 J/EDIV.3	CHK FOR OVERFLOW
	:9848 :0-----	CALL DIV SUBROUTINE
	:9849	
	:9850 :1-----	
	:9851 STATE_STATE+1,	D'END NEG
	:9852 ALU_0=LC, RC[T2]_ALU, Z?;	EXCL OR STATE[00] AS FLAG FOR NEGATE QUOT
	=;END	RC[T2] GETS ABS(D'END <L>), SKIP IF ZERO
	:9853	
	:9854	
	:9855	
	:9856 :0-----	D'END <L> NOT ZERO
	:9857 D_NFT.D,	D'END <H> IS 1'S COMP TO NEGATE D'END
	:9858 J/EDIV.7	GOTO DIV SUBRT
	:9859 :1-----	
	:9860 D_0=D	D'END IS ZERO
	=;END	NEG D'END <H> INSTEAD 1'S COMP OF IT
	:9861	
	:9862	
	:9863 EDIV.7: -----	
	:9864 ALU_LA-D-1, Q_ALU,	CHK FOR OVERFLOW
	:9865 ID[T0]_D, D_0	SAVE D AND CLR IT FOR CONSTRAINT HACK
	:9866	
	:9867 :1-----	
	:9868 D_RC[T2], Q_ID[T0], Q31?;	D = D'END<L>, Q = D'END<H>, OVERFLOW?
	:9869	
	=0** :0-----	OK
	:9870 D_Q, Q_D, J/DIV1X	CALL DIV SUBRT
	:9871	
	:9872	
	:9873 :1-----	
	:9874 D_RC[T1],	OVERFLOW
	:9875 NZ_ALU.V&C_0, J/EDIV.2	Q GETS D'END <L>
	=;END	SET CCL 5 ON D'END <L>
	:9876	

ZZ-ESOAA-124.0 ; ARITH .MIC [600,1204] Integer arithmetic 14-Jan-82 H 5  
; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Fiche 2 Frame H5 Sequence 265  
; ARITH .MIC [600,1204] Integer arithmetic : EDIV Page 264

;9877  
;9878 =011\* ;0----- ; CONSTRANT FOR ALU.N AND PSL.N BRANCHES  
;9879 EDIV.9: ID[T0]\_D, D\_Q, SC\_0(A), ; EXIT CODE - NO OVERFLOW  
;9880 INTRPT\_STROBE, ; QUO = D, REM = Q,  
;9881 STATE\_0(A), J/EMODF.11 ; USE EMODF CODE TO STORE RESULTS  
;9882 ;1----- ; SINCE A PAIR OF LWORDS IS A PAIR OF LWORDS  
;9883 ;1----- ; OVERFLOW  
;9884 D\_RC[T1], N&Z\_ALU.VBC\_0, ; QUOTIENT = DIVIDEND<31:0>  
;9885 J7EDIV.2  
;9886 =0  
;9887 EDIV.Z: ;0----- ; DIVIDE BY 0 COMES HERE  
;9888 Q\_ID[CES], ; GET C.E.S.  
;9889 CALL, J/INDIVO ; GO STICK DIV BY 0 CODE IN CES  
;9890 ;1-----  
;9891 ;1-----  
;9892 ID[T0]\_D, D\_Q, SC\_0(A), ; QUO = D'END<L>, REM = 0,  
;9893 INTRPT\_STROBE, ; USE EMODF CODE TO STORE RESULTS  
;9894 STATE\_0(A), J/EMODF.11 ; SINCE A PAIR OF LWORDS IS A PAIR OF LWORDS  
;9895  
;9896 .LIST ;Re-enable full listing

ZZ-ESOAA-124.0 : INDEX .MIC [600,1204] INDEX.MIC I 5  
: P1W124.MCR [600,1204] MICRO2 1L(03) 14-Jan-82 14-Jan-82 15:30:16 Fiche 2 Frame 15 Sequence 266  
: INDEX .MIC [600,1204] INDEX.MIC VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 265

:9897 .TOC "INDEX.MIC"  
:9898 .TOC "Revision 1.0"  
:9899 : P. R. Guilbault  
:9900

:9901 .NOBIN ..  
:9902 .TOC .. Revision History"  
:9903  
:9904 : 01 Change macro names that deal with condition codes.  
:9905 : 00 Start of history  
:9906

:9907 .BIN  
:9908 .NOLIST ;Disable listing of PCS code for quickie assemblies

:9909 .TOC " Index instruction : INDEX"  
:9910 :  
:9911 : opcode(0A) subscript.rl, low.rl, high.rl, size.rl, indexin.rl,  
:9912 : indexout.wl  
:9913 :  
:9914 :ALGORITHM:  
:9915 :  
:9916 : The operation specified for this instruction is:  
:9917 :  
:9918 : indexin <- {indexin + subscript}\*size;  
:9919 : if {subscript LSS low} or {subscript GTR high}  
:9920 : then {subscript range trap}  
:9921 :  
:9922 : On entry to this routine from C-FORK, the indexin and subscript  
:9923 : operands have been fetched by A-FORK and B-FORK routines. The flow  
:9924 : is as follows:  
:9925 :  
:9926 : 1) Get 'high' limit operand per SPEC subroutine  
:9927 : 2) If 'subscript' operand less than 'low' operand, setup  
:9928 : subscript range trap  
:9929 : 3) Get 'size' operand per SPEC subroutine  
:9930 : 4) If 'subscript' operand less than 'high' operand, setup  
:9931 : subscript range trap  
:9932 : 5) Get 'indexin' operand per SPEC subroutine  
:9933 : 6) Calculate (subscript + indexin) and set condition codes  
:9934 : for next step  
:9935 : 7) If 'size' operand = 1, write above result per WRITE.DEST function  
:9936 : 8) Calculate (subscript + indexin)\*size using MUL.S subroutine  
:9937 : 9) Set condition codes and write result per WRITE.DEST function  
:9938 :  
:9939 :  
:9940 :STORAGE/REGISTER ALLOCATION:  
:9941 :  
:9942 : D-REG 'low' operand on entry  
:9943 : Q-REG 'subscript' operand on entry  
:9944 : ID[CES] Range trap code  
:9945 : ID[T0] temporary  
:9946 : RC[T1] 'size' for MUL.S routine  
:9947 : RC[T2] temporary  
:9948 :  
:9949 :  
:9950 :  
:9951 :3C9: -----  
:9952 : ALU\_Q-D, SET.CC(INST) ; TEST FOR 'LOW' LEQ 'SUBSCRIPT'  
:9953 :  
:9954 :=0\*\*1\* :CALL CONSTRAINT BLOCK FOR SPEC ROUTINE  
:9955 :  
:9956 :0\*1-----  
:9957 :D : MOVE SUBSCRIPT TO D-REG  
:9958 :CALL, J/SPEC : GO GET 'HIGH' OPERAND  
:9959 :  
:9960 :1\*\*1-----: RETURN FROM SPEC ROUTINE  
:9961 :PSL.N? : WAS SUBSCRIPT LESS THAN LOW LIMIT?

U 03C9, 001D,E000,0180,F800,0070,000E

U 000E, 0C00,003D,0180,F800,0000,037E

U 001E, 0000,1A3C,0180,F800,0000,0066

ZZ-ESOAA-124.0 : INDEX .MIC [600,1204] Index instruction 14-Jan-82 K 5  
 : P1W124.MCR 600,1204] MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : INDEX .MIC [600,1204] Index instruction : INDEX Sequence 268  
 Page 267

U 0066, 0C01,003D,31F0,2D90,0000,0591	:9962 =0011* ;CALL CONSTRAINT BLOCK FOR SPEC AND PSL.N BRANCH(BEN/PSL)	
	:9963	
	:9964 :0011*-----; *** SUBSCRIPT RANGE TRAP DETECTED ***	
	:9965 Q_ID[CES]. : GET CP ERR/STATUS REG	
	:9966 D_Q. : SAVE Q-REG IN D-REG	
	:9967 RC[T2]_D, : SAVE D-REG IN RC STACK	
	:9968 CALL, J/INDEX.9 : GO SET EXCEPTION TRAP CODE & RETURN8	
	:9969	
	:9970 :0111*-----; *** LOW LIMIT OK, GO GET SIZE OPERAND ***	
	:9971 ALU_D-Q, SET.CC(INST). : TEST FOR 'HIGH' > 'SUBSCRIPT'	
	:9972 D_Q. : MOVE SUBSCRIPT TO D-REG	
	:9973 CALL, J/SPEC : GO GET SIZE (SUBSCRIPT/Q-REG ON RETURN)	
	:9974	
U 006E, 0C1D,C001,0180,F800,0070,037E	:9975 =1111* ;1111*-----; *** RETURN10/12 FROM SPEC ***	
	:9976 ALU_D-K[.1], CLK.UBCC, : TEST 'SIZE' FOR EQ 1	
	:9977 PSL.N? : WAS 'HIGH' > 'SUBSCRIPT'	
	:9978	
U 007E, 0019,1A00,0580,F800,0010,01A6	:9979 =0011* ;CALL CONSTRAINT BLOCK FOR SPEC AND PSL.N BRANCH(BEN/PSL)	
	:9980	
	:9981 :0011*-----; *** SUBSCRIPT RANGE TRAP DETECTED ***	
	:9982 Q_ID[CES]. : GET CP ERR/STATUS REG	
	:9983 D_Q. : SAVE Q-REG IN D-REG	
	:9984 RC[T2]_D, : SAVE D-REG IN RC STACK	
	:9985 CALL, J/INDEX.9 : GO SET EXCEPTION TRAP CODE & RETURN8	
	:9986	
U 01A6, 0C01,003D,31F0,2D90,0000,0591	:9987 :0111*-----; *** HIGH LIMIT OK, GO GET INDEX OPERAND ***	
	:9988 ID[0]_D, : SAVE MULTIPLIER(SIZE)	
	:9989 RC[T1]_D, : SET UP T1 FOR MULTIPLY ROUTINE	
	:9990 D_Q. : MOVE SUBSCRIPT TO D-REG	
	:9991 CALL, J/SPEC : GO GET INDEXIN (SUBSCRIPT/Q-REG ON RETURN)	
	:9992	
U 01AE, 0C01,003D,C180,3D88,0000,037E	:9993 =1111* ;1111*-----; *** RETURN10/12 FROM SPEC ***	
	:9994 D&Q_D+Q, NBZ_ALU.V&C_0, : ADD SUBSCRIPT TO INDEXIN	
	:9995 SC_R[.FF], : START SETUP OF 100	
	:9996 Z? : WAS SIZE EQ TO 1?	
	:9997	
	:9998	
	:9999	
U 01BE, 081D,0114,49C0,F800,00D4,6390	:10000 =0 ;ALU CC<Z> EQ 0?(BEN/Z)	
	:10001	
	:10002 :0-----; *** SIZE OPERAND NOT EQ 1 ***	
	:10003 SC_SC+1. : 100 ->SC	
	:10004 J/INDEX.3	
	:10005	
	:10006 :*****	
	:10007 * Patch no. 061, PCS 0390 trapped to WCS 1187 *	
	:10008 :*****	
	:10009 :*****	
	:10010 :1-----; *** SIZE OPERAND EQ 1 ***	
	:10011 WRITE.DEST : WRITE RESULT BY GOING TO C-FORK AWRD:	
U 0391, F000,003F,01F0,F847,0000,0300	:10012	

ZZ-ESOAA-124.0 ; INDEX .MIC [600,1204] Index instruction 14-Jan-82  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 Fiche 2 Frame L5  
 ; INDEX .MIC [600,1204] Index instruction : INDEX VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124

Sequence 269 Page 268

L 5

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:10012 =0110 ;CALL CONSTRAINT BLOCK FOR MUL.S ROUTINE
:10013
:10014 INDEX.3:;0110-----;
:10015 CALL, J/MUL.S ; GO DO (INDEXIN+SUBSCRIPT)*SIZE
:10016
:10017 ;0111-----; RETURN FROM MUL.S
:10018 ALU.D, NZ_ALU.VBC_0, ; SET CONDITION CODES FOR RESULT
:10019 WRITE.DEST ; WRITE RESULT BY GOING TO C-FORK @ WRD:
:10020
:10021 ;1110-----; RETURN FROM MUL.S
:10022 ALU.D, NZ_ALU.VBC_0, ; SET CONDITION CODES FOR RESULT
:10023 WRITE.DEST ; WRITE RESULT BY GOING TO C-FORK @ WRD:
:10024
:10025 ;1111-----; RETURN FROM MUL.S
:10026 ALU.D, NZ_ALU.VBC_0, ; SET CONDITION CODES FOR RESULT
:10027 WRITE.DEST ; WRITE RESULT BY GOING TO C-FORK @ WRD:
:10028
:10029 INDEX.9:-----
:10030 Q_Q.OR.K[.30] ;
:10031
:10032 -----;
:10033 Q_D,
:10034 D_Q.OR.K[.40] ; RESTORE Q-REG
:10035
:10036 -----;
:10037 D_RC[T2],
:10038 ID[CES]_D, ; RESTORE D-REG
:10039 RETURN8 ; SET SUBSCRIPT RANGE TRAP FLAG
:10040
:10041 .LIST ;RETURN AND CONTINUE INSTRUCTION
:10041 .LIST ;Re-enable full listing

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ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204]  
: P1W124.MCR 600,1204]  
: FLOAT .MIC [600,1204]

FLOAT.MIC  
MICR02 1L(03)  
FLOAT.MIC

M 5  
14-Jan-82

14-Jan-82 15:30:16

VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124

Fiche 2 Frame M5

Sequence 270  
Page 269

:10042 .TOC 'FLOAT.MIC'  
:10043 .TOC 'Revision 2.14'  
:10044 ; P. R. Guilbault  
:10045

:10046 .NOBIN ..  
:10047 .TOC .. Revision History"  
:10048 ..  
:10049 : 02 Fix POLY FPD problem that backs up the regs on interrupt  
:10050 : Add general WCS region  
:10051 : Convert EMODF to floating faults  
:10052 : Convert POLYF/D to floating faults  
:10053 : Fix (MUL,DIV)F2 destination register when floating fault.  
:10054 : Fix POLYF when argument or partial product is zero.  
:10055 : Remove absolute jumps.  
:10056 : Add CVTRDL.G tag for G&h  
:10057 : Change macro names that deal with conditions codes.  
:10058 : 01 Delete FLOATW.MIC and put code here. Use .REGION to get it into WCS.  
:10059 : FLOATW 00 Create this file by merging MULD.MIC, EMOD.MIC, POLY.MIC  
:10060 : FLOATW Remove macros that were defined MULD.MIC and put in MACRO.MIC  
:10061 : FLOATW Start of history  
:10062 : 00 Add LIST to enable listing of WCS code for WCS only listing  
:10063 : Delete DBL.MIC, CVT2F.MIC, CVTFI2.MIC, ACBFD2.MIC and put code here.  
:10064 : Start of history  
:10065 ..  
:10066 .BIN  
:10067 .NCLIST ;Disable listing of PCS code for quickie assemblies

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1WT24.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : CMPF

N 5

Fiche 2 Frame NS

Sequence 271

Page 270

	:10068 .TOC " F & D floating point : CMPF"	
	:10069	
	:10070 :THE SPECIFIER 1 OPERAND IS COMPARED WITH THE SPECIFIER 2 OPERAND.	
	:10071 :PSL<ND> <- SP1 LSS SP2	
	:10072 :PSL<Z> <- SP1 EQL SP2	
	:10073 :PSL<V> <- 0	
	:10074 :PSL<C> <- 0	
	:10075	
	:10076 :ENTER HERE FROM DP2.WITH D CONTAINS DST, Q CONTAINS SRC.	
	:10077	
	:10078 : THE COMPARISON IS DONE IN A SIGN-INDEPENDENT MANNER; THE	
	:10079 : CONDITION CODES ARE SET FROM THE SOURCE OR FROM THE	
	:10080 : NEGATED DESTINATION, WHICHEVER IS HIGHER IN MAGNITUDE.	
	:10081 : IF THE SIGNS ARE DIFFERENT, THE TWO TESTS ARE THE SAME (OF COURSE)	
	:10082 : SO NO MAGNITUDE COMPARISON IS DONE.	
	:10083	
	:10084 : MAGNITUDES ARE COMPARED BY COMARING THE EXPONENTS, AND THEN	
	:10085 : COMPARING THE FRACTIONS IF THE EXPS ARE EQUAL.	
	:10086 : THE ONLY SPECIAL CASE IS THAT BOTH EXPONENTS = 0 MEANS EQUALITY.	
	:10087	
	:10088 3C1:	
	:10089 CMPF:	
U 03C1, 001D, 0038, 01C9, F980, 0998, 65D4	:10090 ALU Q(B), : GET SRC AND DEST EXPONENTS	
	:10091 SC ALU(EXP), FE_D(EXP),	
	:10092 RC[T0] ALU,	: SAVE AND UNPACK SRC
	:10093 Q_ALU(FRAC), SS_ALU15,	
	:10094 CLK.FLT.OPR, CLK.UBCC	: CHECK FOR -0 AND SET CC'S ON EXPS
	:10095	
	:10096	
	:10097 R[R15], D, : SAVE DST, UNPACK DST, GET EXP DIFF	
	:10098 D_D(FRAC), EALU SC-FE,	
U 05D4, 0901, 123C, 0185, FAF8, 0810, A4E9	:10099 SS_SS.XOR.ALU15&SD_ALU15, : REMEMBER IF SIGNS DIFFERENT	
	:10100 CLK.FLT.OPR, CLK.UBCC, EALU?	: SET CC ON EXP DIFF, TEST EXPS=0
	:10101	
U 04E9, C018, C020, 4580, A7C, 4070, 0062	:10102 :1001-----	
	:10103 ALU_R[R15].XOR.K[.8000], : SET CONDITION CODES FROM -SRC2	
	:10104 SET(CC(INST)),	
	:10105 CLR.IB.OPC, PC_PC+1, J/IRD	
	:10106	
U 04EB, 001D, 3200, 0180, F800, 0010, 0592	:10107	
	:10108 ALU_Q-D, CLK.UBCC, : EXPS<>0 - CMP FRACS, TST EXP DIFF	
	:10109 EALU?, J/CKDIFO	
	:10110	
U 04ED, C018, C038, 1980, F804, 4070, 0062	:10111	
	:10112 ALU_K[ZERO], SET(CC(INST)), : DST, SRC = 0	
	:10113 CLR.IB.OPC, PC_PC+1, J/IRD	
	:10114	
U 04EF, C010, C038, 0180, F904, 4070, 0062	:10115	
	:10116 ALU_RC[T0], SET(CC(INST)), : DST = 0, SRC .NE. 0	
	:10117 CLR.IB.OPC, PC_PC+1, J/IRD	: SET CC'S FROM SRC

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 IL(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Sequence 272  
 ; FLOAT .MIC [600,1204] F & D floating point : CMPF Page 271

B 6

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;10118 =0010
;10119 CKDIFO: ;0010-----
;10120 ALU.RC[T0].SET.CC(INST),
;10121 CLR.IB.OPC,PC_PC+1,J/IRD ;SRC > DST
;10122
;10123 ;0011-----
;10124 ALU.R([T0].SET.CC(INST),
;10125 CLR.IB.OPC,PC_PC+1,J/IRD ;SRC > DST
;10126
;10127 ;0110-----
;10128 ALU?, J/CHECKF ;SRC(EXP)=DST(EXP) - TEST FRAC DIFF
;10129
;10130 ;0111-----
;10131 ALU.RC[T0].SET.CC(INST),
;10132 CLR.IB.OPC,PC_PC+1,J/IRD ;DIFF SIGNS: CC SET AS SRC
;10133
;10134 ;1010-----
;10135 ALU.R[R15].XOR.K[.8000], ;DST > SRC
;10136 SET.CC(INST),
;10137 CLR.IB.OPC,PC_PC+1,J/IRD ;
;10138
;10139 ;1011-----
;10140 ALU.R[R15].XOR.K[.8000], ;DST > SRC
;10141 SET.CC(INST),
;10142 CLR.IB.OPC,PC_PC+1,J/IRD ;
;10143 =
  
```

ZZ-ESOAA-124.0 ; FLOAT .MIC [6(0,1204] F & D floating point 14-Jan-82 Fiche 2 Frame C6 Sequence 273  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 272  
 : FLOAT .MIC [600,1204] F & D floating point : ADDF, SUBF

C 6

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:10144 .TOC   "      F & D floating point : ADDF, SUBF"
:10145
:10146 :ADD/2/SUBF2 Short literal, Register
:10147 :HERE FROM IRD, WITH LA CONTAINS SP2 (DST), AND Q CONTAINS SP1 (SRC).
:10148 040:
:10149
:10150 :-----:ALU_Q, :SETUP EXP
:10151 D_Q,SC_Q(EXP),SS_ALU15,
:10152 CRK.FLT.OPR
:10153
:10154
:10155 :ADD/2/SUBF2 Register, Register
:10156 :HERE FROM IRD, WITH LA CONTAINS SP2 (DST), AND D CONTAINS SP1 (SRC).
:10157 044:
:10158 ADDF: :0****0100-----:
:10159 Q_D,RC[T0]-LA, :SAVE DST OPERAND
:10160 D_LA(FRAC),SC_NABS(SC-FE), :UNPACK DST FP, GET EXP DIFFERENCE
:10161 SGN/ADD.SUB, :SS +/- INDICATOR, SET SD
:10162 CRK.FLT.OPR,CLK.LBCC, :RSV OPD FAULT IF -0, SET ALUS CC
:10163 CALL,EALU?,J/ADDFX :CHECK FOR 0 EXPS
:10164
:10165 144: :1****0100-----:RET FOR RESULT=0
:10166 R(SP1)_K[ZERO],
:10167 EALU_K[ZERO],SET_CC(INST),
:10168 CLR.IB0-1,PC_PC+2,J/IRD
:10169
:10170 14C:
:10171 ADDFDN: :1****1100-----:RET FOR ADDF2/SUBF2
:10172 EALU_SC,R(SP1)_PACK.FP, :PACK RESULT
:10173 SET_CC(INST), :SET COND CODES
:10174 CLR.IB0-1,PC_PC+2, :UPDATE PC, POP IB
:10175 SC?,J/EXPCKR :CK IF UNDERFL OR OVFL
:10176
:10177 14D: :1****1101-----:RET FOR ADD/SUBF2, NORMALIZE AFTR ROUND
:10178 D_D.RIGHT,SC_SC+1,J/ADDFDN :SHIFT RIGHT, ADD 1 TO EXP
:10179
:10180
:10181
:10182 14E: :1****1110-----:RET FOR SR<=0 OR DEST=0, OR
:10183 EALU_SC,R(SP1)_PACK.FP, :RET FOR ADDF3/SUBF3
:10184 SET_CC(INST), :PACK RESULT FOR *-R-R MODE
:10185 CLR.IB0-1,PC_PC+2, :SET COND CODES
:10186 SC?,J/EXPCKR :UPDATE PC, POP IB
:10187 :CK IF UNDERFL OR OVFL
:10188 14F: :1****1111-----:RET FOR ADD/SUBF3, NORMALIZE AFTR ROUND
:10189 D_D.RIGHT,SC_SC+1,J/ADDFDN :SHIFT RIGHT, ADD 1 TO EXP
  
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U 0040, 0C01,203C,0181,F800,0888,6044  
 U 0044, 0900,123D,01E6,F980,0890,E4<sup>F9</sup>  
 U 0144, 4018,C038,1980,F8C5,4074,6062  
 U 014C, 4008,D438,0180,F8C5,4070,05D1  
 U 014E, 0600,003C,0180,F800,0080,C14C  
 U 014E, 4008,D438,0180,F8C5,4070,05D1  
 U 014F, 0600,003C,0180,F800,0080,C14C

D 6

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 Fiche 2 Frame 06 Sequence 274  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 273  
 ; FLOAT .MIC [600,1204] F & D floating point : ADDF, SUBF

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:10190 :ADD3/SUBF3 ****, Register, Register
:10191 :ENTER HERE AT B.FORK WITH D HAS SP1 OPERAND, LA HAS SP2 OPERAND.
:10192 :244:
:10193 :-----:
:10194 :SC_D(EXP)(B) :GET EXP'S, SS
:10195 :FE_LA(EXP),SS_ALU15,
:10196 :CHR.FLT.OPR,CLK.UBC,C,J/ADDF :LOAD ALU'S U BRANCH COND CODES
:10197 :
:10198 :
:10199 :
:10200 :ADD3/SUBF3 ****, Short literal, Register
:10201 :ENTER HERE AT B.FORK WITH D HAS SP1 OPERAND, Q SP2 OPERAND.
:10202 :240:
:10203 :-----:
:10204 :SC_D(EXP)(B), :ADDF MEM MODE
:10205 :FE_Q(EXP),SS_ALU15,
:10206 :D_Q,Q,D,
:10207 :CLK.UBC,C :SWAP D, Q
:10208 :LOAD ALU'S U BRANCH COND CODES
:10209 =0*****1100
:10210 :0*****1100----:
:10211 :RC[T0],D,D_D(FRAC), :D=SRC, RC[T0]=DST
:10212 :SC_NABS(SC-FE),
:10213 :SGN/ADD.SUB,
:10214 :CHK.FLT.OPR,CLK.UBC,C,
:10215 :CALL,EALU?,J/ADDFX :SS +/- INDICATOR, SD GETS DST SGN
:10216 :
:10217 =1*****1100
:10218 :1*****1100----:FAULT IF NEG FP 0
:10219 :R(SP1)_K[Z^C],
:10220 :EALU_K[ZERO],SET.CC(INST),
:10221 :CLR.IBO-1,PC_PC+2,J/IRD :RESULT 0
:10222 :GOTO NEXT INST
:10223 :
:10224 ADDFDB: 1*****1110----:RETURN HERE WHEN DONE
:10225 :EALU_SC,R(SP1)_PACK.FP, :PACK RESULT
:10226 :SET.CC(INST),
:10227 :CLR.IBO-1,PC_PC+2,
:10228 :SC?,J/EXPCKR :CK IF UNDEPFL OR OVFL
:10229 :
:10230 :1*****1111----:
:10231 :D_D.RIGHT,SC_SC+1,J/ADDFDB :SHIFT RIGHT, ADD 1 TO EXP
:10232 =

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U 0244, 001C,2038,0181,F800,099B,6044

U 0240, 0C1D,2038,01E1,F800,019B,607C

U 007C, 0901,123D,0186,F980,0890,E4F9

U 017C, 4018,0038,1980,F8C5,4074,6062

U 017E, 4008,D438,0180,F8C5,4070,05D1

U 017F, 0600,003C,0180,F800,0080,C17E

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : ADDF, SUBF

E 6

Fiche 2 Frame E6

Sequence 275

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U 022F. 001C.2038.0181,F800,099B,603A :10233 ;ADDF2/SUBF2 Register destination  
 :10234 ;ENTER HERE AT B.FORK, WITH D CONTAINS SP1 OPERAND, AND LA SP2 OPERAND.  
 :10235 22F:  
 :10236 :-----  
 :10237 SC\_D(EXP)(B),FE\_LA(EXP), :GET EXP'S  
 :10238 SS\_ALU15,  
 :10239 CHR.FLT.OPR,CLK.UBCC :  
 :10240 :  
 :10241 =0\*\*\*\*1010  
 :10242 :0\*\*\*\*1010-----:2-OPR: UPC[1] IS DON'T CARE  
 :10243 O\_D,RC[T0].LA. :SAVE DST OPD  
 :10244 D\_LA(FRAC).SC\_NABS(SC-FE). :UNPACK DST FP, GET EXP DIFFERENCE  
 :10245 SGN/ADD.SUB, :SS +/- INDICATOR, SET SD  
 :10246 CHK.FLT.OPR,CLK.UBCC, :RSV OPD FAULT IF -0, SET ALUS CC  
 :10247 CALL,EALU?,J/ADDFX :CHECK FOR 0 EXPS  
 :10248 :  
 :10249 =1\*\*\*\*1010  
 :10250 :-----  
 :10251 R(PRN) K[ZERO],  
 :10252 EALU K[ZERO],SET.CC(INST), :RESULT 0  
 :10253 CLR.IB.OPC,PC\_PC+1,J/IRD :GOTO NEXT INST  
 :10254 :  
 :10255 =1\*\*\*\*1110  
 :10256 ADDFDX: :1\*\*\*\*1110-----  
 :10257 EALU SC,R(PRN)\_PACK.FP. :PACK RESULT  
 :10258 SET.CC(INST). :SET COND CODES  
 :10259 CLR.IB.OPC,PC\_PC+1. :UPDATE PC, POP IB  
 :10260 SC?,J/EXPCKP :CK IF UNDERFL OR OVFL  
 :10261 :  
 :10262 :1\*\*\*\*1111-----  
 :10263 D\_D.RIGHT,SC\_SC+1,J/ADDFDX :SHIFT RIGHT, ADD 1 TO EXP  
 :10264 =

U 003A. 0900.123D.01E6,F980,0890,E4F9

U 013A. C018.C038.1980,F8DC,4074,6062

U 013E. C008.D438.0180,F8DC,4070,05E1

U 013F. 0600.003C.0180,F800,0080,C13E

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 F 6  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Sequence 276  
 : FLOAT .MIC [600,1204] F & D floating point : ADDF, SUBF

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U 038E, 001D,0038,0181,F800,099B,60D8      Fiche 2 Frame F6  
 :10265 ;ADDF2/SUBF2      Memory destination  
 :10266 ;ADDF3/SUBF3      Register/Memory destination  
 :10267  
 :10268 ;ENTER HERE AT C.FORK  
 :10269 ; TO MEMORY MODE INSTRUCTIONS  
 :10270 ; WITH D CONTAINS DST (OR SP2), Q CONTAINS SRC (OR SP1) OPERANDS  
 :10271 38E:  
 :10272 ADDFA: ;-----  
 :10273      SC\_Q(EXP)(B),FE\_D(EXP),      ;ADDF MEM MODE  
 :10274      SS\_ALU15,      ;  
 :10275      CHR.FLT.OPR,CLK.UBCC      ;  
 :10276  
 :10277 =0\*\*\*\*1000  
 :10278      :0\*\*\*\*1000-----  
 :10279      RC[T0] D,D\_D(FRAC),      ;D=SRC, RC[T0]=DST, SRC-DST EXP  
 :10280      SC\_NABS(SC=FE),  
 :10281      SGN/ADD.SUB,      ;SS +/- INDICATOR, SD GETS DST SGN  
 :10282      CHK.FLT.OPR,CLK.UBCC,      ;FAULT IF NEG FP 0  
 :10283      CALL,EALU?,J/ADDFX      ;  
 :10284  
 :10285 =1\*\*\*\*1000  
 :10286 WR.Z: ;1\*\*\*\*1000-----  
 :10287      EALU\_K[ZERO],      ;WRITE RESULT FLOAT 0  
 :10288      D\_K[ZERO],SET.CC(INST),  
 :10289      WRITE.DEST,J/WRD      ;  
 :10290  
 :10291 =1\*\*\*\*1100  
 :10292 ADDFDA: ;1\*\*\*\*1100-----  
 :10293      EALU\_SC,D\_PACK.FP,      ;ADDF2/SUBF2: PACK RESULT  
 :10294      SET.CC(INST),  
 :10295      SC?,J/EXPCKM      ;CK IF UNDERFL OR OVFL  
 :10296  
 :10297 ;1\*\*\*\*1101-----  
 :10298      D\_D.RIGHT,SC\_SC+1,J/ADDFDA      ;SHIFT RIGHT, ADD 1 TO EXP  
 :10299  
 :10300 ADDFDF: ;1\*\*\*\*1110-----  
 :10301      EALU\_SC,D\_PACK.FP,      ;ADDF3/SUBF3: PACK RESULT  
 :10302      SET.CC(INST),  
 :10303      SC?,J/EXPCK      ;CK IF UNDERFL OR OVFL  
 :10304  
 :10305 ;1\*\*\*\*1111-----  
 :10306      D\_D.RIGHT,SC\_SC+1,J/ADDFDE      ;SHIFT RIGHT, ADD 1 TO EXP  
 :10307 =

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 G 6  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Fiche 2 Frame G6 Sequence 277  
 : FLOAT .MIC [600,1204] F & D floating point : ADDF, SUBF Page 276

	:10308	;HERE BEGINS THE EXPONENT CHECKS OF FLOATING ADD/SUBTRACT	
	:10309	;ENTER HERE BRANCHING ON EALU Z AND SC .NE. 0	
	:10310	; WITH THE FIRST OPERAND EXPONENT IN SC AND PACKED IN Q,	
	:10311	; THE SECOND OPERAND EXPONENT IN FE, AND UNPACKED FRACTION IN D.	
	:10312	; SC SHOULD BE BEING LOADED WITH NABS(SC-FE).	
	:10313		
	:10314	=1001 :-----	:EALU Z=0, SC .EQ. 0 (SRC IS ZERO)
U 04F9, 0501,203E,0180,F800,0881,010E	:10315	ADDFX: ALU_Q,CHK.FLT.OPR.	;CHECK FOR SRC RESERVED OPERAND
	:10316	D_D.LEFT,SI/ZERO,	;NORMALIZE FRACTION FROM DEST
	:10317	SC_FE,	;GET DEST EXPONENT
	:10318	RETURN10E	;SEND BACK DEST AS RESULT
	:10319		
	:10320	:-----	:EALU Z=0, SC .NEQ. 0 (NORMAL CASE)
U 04FB, 0001,323C,C5C8,3EF8,0000,05A2	:10321	R[IR15]_Q,Q_Q(FRAC),	;EXPS NE 0: UNPACK SRC FP
	:10322	ID[CT1]_D,	;SAVE DST FRAC
	:10323	EALU?,J/ADDFSH	;COMPARE SRC - DST EXPS
	:10324		
U 04FD, 0F01,203E,1980,F800,0884,6100	:10325	:-----	:EALU Z=1, SC .EQ. 0 (BOTH ZERO)
	:10326	ALU_Q,CHK.FLT.OPR.	;MAKE SURE SRC ISN'T RESERVED
	:10327	D_0,SC_K[ZERO],	;CLEAR RESULT
	:10328	RETURN00	
	:10329		
	:10330	:-----	:EALU Z=1, SC .NEQ. 0 (DEST IS ZERO)
U 04FF, 0901,203C,0184,F800,0108,64F9	:10331	D_Q(FRAC),FE_Q(EXP),	;UNPACK SRC AS RESULT
	:10332	SD_SS,	;SRC SIGN XOR IR1 IS RESULT SIGN
	:10333	J/ADDFX	;NOW GO PACK IT UP AGAIN

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 ; FLOAT .MIC [600,1204] F & D floating point : ADDF/SUBF ROUTINE

H 6

Fiche 2 Frame H6

Sequence 278

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;10334 .TOC   "      F & D floating point : ADDF/SUBF ROUTINE"
;10335
;10336 :ROUTINE SHARED BY DIFFERENT MODES OF ADDF, SUBF: ALSO POLYF AND ACBF
;10337
;10338 :ENTER HERE WITH :      D      = FRAC(DST)
;10339          ID[T1] = FRAC(DST)
;10340          FE     = EXP(DST)
;10341          Q      = FRAC(SRC)
;10342          R[15] = SRC
;10343          SC    = NABS(EXP DIFF)
;10344          SS    = SIGN(SRC).xor.SIGN(DST).xor.IR<1>
;10345          SD    = SIGN(DST)
;10346
;10347 : NOTE: EXP DIFFERENCE OF UP TO 31 IS SIGNIFICANT BECAUSE OF POLYF USAGE
;10348
;10349 =0010
;10350 ADDFSH: :0010-----; SRC.GTR.DST, SS = 0(ADD)
;10351 EALU SC+K[.1F],CLK.UBCC,      ; SET UP EALU<ND> TO CHECK SHIFT RANGE
;10352 Q_0,J/AL0                  ; Q GETS POSITIVE SIGN FOR DAL SHIFT
;10353
;10354 :0011-----; SRC.GTR.DST, SS = 1(SUB)
;10355 EALU SC+K[.1F],CLK.UBCC,      ; SET UP EALU<ND> TO CHECK SHIFT RANGE
;10356 D_0-D,SD_NOT.SD,J/DF0       ; COMPLIMENT FRAC(DST) TO DO SUB
;10357
;10358 :0110-----; SRC.EQL.DST, SS = 0(ADD)
;10359 D_D+Q,Q_0,SC_FE,            ; ADD 2 ALIGNED FRACS
;10360 CLK.UBCC,J/ADDFPK         ;
;10361
;10362 :0111-----; SRC.EQL.DST, SS = 1(SUB)
;10363 D_D-Q,Q_0,SC_FE,            ; SUBTRACT 2 ALIGNED FRACS
;10364 CLK.UBCC,J/NEGCK          ;
;10365
;10366 :1010-----; DST.GTR.SRC, SS = 0(ADD)
;10367 EALU SC+K[.1F],CLK.UBCC,      ; SET UP EALU<ND> TO CHECK SHIFT RANGE
;10368 D_Q,Q_0,J/AL1              ; D GETS SRC FRAC, CLR Q FOR DAL SHF
;10369
;10370 :1011-----; DST.GTR.SRC, SS = 1(SUB)
;10371 EALU SC+K[.1F],CLK.UBCC,      ; SET UP EALU<ND> TO CHECK SHIFT RANGE
;10372 D_0-Q,J/DF1                ; D GETS (-SRC FRAC) FOR SUBTRACT
;10373 =
;10374 AL0: -----
;10375          D_DAL.SC,
;10376          Q_R[R15](FRAC),FE_R[R15](EXP), ; ALIGN DST FRAC
;10377          EALU?,J/DSTAPO             ; Q, FE GET SRC FRAC, EXP
;10378
;10379 DF0: -----
;10380          Q_0-K[.1],J/AL0           ; GO CHECK SHIFT RANGE
;10381
;10382 AL1: -----
;10383          D_DAL.SC,
;10384          Q_ID[T1],                ; ALIGN SRC FRAC
;10385          EALU?,J/SRCAP0          ; GET BACK DST FRAC
;10386
;10387 DF1: -----
;10388          Q_0-K[.1],J/AL1           ; GO CHECK SHIFT RANGE
;10389
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ZZ-ES0AA-124.0 : FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : ADDF/SUBF ROUTINE

I 6

Fiche 2 Frame I6

Sequence 279

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U 0527, 081D,0014,01F8,F800,0091,05C3

:10389 =0111  
 :10390 DSTAPO: :0111----- ; EALU<ND> = 0, SHIFT WAS LEQ 31  
 :10391 D\_D+Q,Q,0,SC\_FE, ; ADD 2 ALIGNED FRACS  
 :10392 C[K.UBCC,J/ADDFPK ;  
 :10393  
 :10394 :1111----- ; EALU<ND> = 1, SHIFT WAS GTR 31  
 :10395 ALU\_Q+K[ZERO],  
 :10396 D\_A[U.LEFT,SI/ZERO,  
 :10397 C[K.UBCC,SC\_FE,J/ROUND1 ; DST APPROX 0 W.R.T. SRC  
 :10398 CLR ALU C31  
 :10399 =0111  
 :10400 SRCAP0: :0111----- ; EALU<ND> = 0, SHIFT WAS LEQ 31  
 :10401 D\_D+Q,Q,0,SC\_FE, ; ADD 2 ALIGNED FRACS  
 :10402 C[K.UBCC,J/ADDFPK ;  
 :10403  
 :10404 :1111----- ; EALU<ND> = 1, SHIFT WAS GTR 31  
 :10405 SC\_FE,D\_Q,LEFT,SI/ZERO,K[.80] ; SRC APPROX 0 WRT DST, SET CC  
 :10406  
 :10407  
 :10408 D\_D+K[.80],CLK.UBCC,J/ROUND1 ; THE ROUNDING IS FOR POLYF  
 :10409  
 :10410  
 :10411 NEGCK: -----  
 :10412 ALU\_0+K[.1]+1,CLK.UBCC,ALU? ; CK IF NEG RESULT  
 :10413 =0011  
 :10414 ADDFPK: :0011-----  
 :10415 SC\_SC-SHF.VAL,D\_DAL.NORM, ; NORMALIZE FRAC  
 :10416 K[.80],J/ROUND ; SET UP FOR CONST -81 V:1 MASK  
 :10417  
 :10418 :0111-----  
 :10419 D\_K[ZERO],SC\_K[ZERO], ; RESULT 0  
 :10420 RETURN100  
 :10421  
 :10422 :1011-----  
 :10423 D\_0-D,SD\_NOT.SD,J/ADDFPK ; GET ABS(DIFF) FOR FRAC  
 :10424  
 :10425  
 :10426 ROUND: :-----  
 :10427 D\_D+K[.80],SC\_SC+1,CLK.UBCC ; D\_D+80 FOR ROUNDING  
 :10428  
 :10429 ROUND1: :-----  
 :10430 ALU\_R(SP1)+K[ZERO].RLOG, ; SAVE REG # FOR R-R OVERFLOWS  
 :10431 ALU?,RETURN10C ; CHECK IF RENORMALIZE AGAIN

U 0537, 081D,0014,01F8,F800,0091,05C3

U 053F, 0821,203C,4180,F800,0081,05F2

U 05F2, 0819,0014,4180,F800,0010,0621

U 0604, 001B,1B10,0580,F800,0010,05C3

U 05C3, 0E00,003C,4180,F800,008C,A611

U 05C7, 0818,003A,1980,F800,0084,6100

U 05CB, 081F,2000,0183,F800,0000,05C3

U 0611, 0819,0014,4180,F800,0090,C621

U 0621, 0018,1B1A,1980,F840,0000,010C

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 ; FLOAT .MIC [600,1204] F & D floating point : ADDF/SUBF ROUTINE

J 6

Fiche 2 Frame J6

Sequence 280

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:10432 :CLEANUP FOR SL/R-R, \*\*SL/R-R ADDS. RESULT ALREADY STORED.  
 :10433 :COME HERE WITH BEN/SC TO TEST FOR OVERFLOW AND UNDERFLOW.  
 :10434 :THE REGISTER NUMBER OF THE DESTINATION IS LOST HERE, AND MUST  
 :10435 :BE RECONSTRUCTED FROM THE RLOG STACK IF OVER/UNDERFLOW EXISTS.  
 :10436 =0001  
 :10437 EXPCKR: :0001-----  
 :10438 RC[T0] K[ZERO], ;ZERO EXP. UNDERFLOW, SET TRAP STACK  
 :10439 CALL,J7UNDRFL ;SET CES FOR UNDERFLOW  
 :10440  
 :10441 :0011----- ;01 TO FF FOR EXP, OK  
 :10442 IRD  
 :10443  
 :10444 :0101-----  
 :10445 RC[T0] K[ZERO], ;NEG EXP. UNDERFLOW, SET TRAP STACK  
 :10446 CALL,J7UNDRFL ;SET CES FOR UNDERFLOW  
 :10447  
 :10448 :0111-----  
 :10449 RC[T0] K[.8000], ;> FF EXP. OVERFLOW, SET TRAP STACK  
 :10450 CALL,J7OVFL ;SET CES FOR OVERFLOW  
 :10451 =1111  
 :10452 :1111-----  
 :10453 D\_RLOG.RIGHT ;RETURN HERE FOR UNDERFLOW, OVERFLOW  
 :10454  
 :10455 :-----  
 :10456 SC\_D(EXP)(A), D\_RC[T0] ;PUT REG # IN SC, GET RESULT  
 :10457  
 :10458 :-----  
 :10459 R(SC) J/IRD ;STORE IT AND GET OUT  
 :10460  
 :10461  
 :10462 :CLEANUP FOR \*-R ADDS. RESULT ALREADY STORED IN R(PRN).  
 :10463 :COME HERE WITH BEN/SC TO TEST FOR UNDERFLOW AND OVERFLOW.  
 :10464 =0001  
 :10465 EXPCKP: :0001-----  
 :10466 R(PRN) K[ZERO], ;ZERO EXP. UNDERFLOW, SET TRAP STACK  
 :10467 CALL,J7UNDRFL ;SET CES FOR UNDERFLOW  
 :10468  
 :10469 :0011-----  
 :10470 IRD ;01 TO FF FOR EXP, OK  
 :10471  
 :10472 :0101-----  
 :10473 R(PRN) K[ZERO], ;NEG EXP. UNDERFLOW, SET TRAP STACK  
 :10474 CALL,J7UNDRFL ;SET CES FOR UNDERFLOW  
 :10475  
 :10476 OVFLP: :0111-----  
 :10477 R(PRN) K[.8000], ;> FF EXP. OVERFLOW, SET TRAP STACK  
 :10478 CALL,J7OVFL ;SET CES FOR OVERFLOW  
 :10479 =1111  
 :10480 :1111-----  
 :10481 IRD ;RETURN HERE FOR UNDERFLOW, OVERFLOW

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:10482 :CLEANUP FOR *** ADDS, RESULT IN D, ADDRESS IN VA.
:10483 :COME HERE WITH BEN/SC TO TEST FOR UNDERFLOW AND OVERFLOW.
:10484 =0001
:10485 EXPCKM: :0001-----
:10486 D 0 ;ZERO EXP. UNDERFLOW, SET TRAP STACK
:10487 CALL,J/UNDRFL ;GOTO SET CES FOR UNDERFLOW
:10488
:10489 :0011-----
:10490 CACHE D[INST.DEP]
:10491 CLR.IB.OPC,PC_PC+1,J/IRD ;01 TO FF FOR EXP, OK
:10492
:10493 :0101-----
:10494 D 0 ;NEG EXP. UNDERFLOW, SET TRAP STACK
:10495 CALL,J/UNDRFL ;GOTO SET CES FOR UNDERFLOW
:10496
:10497 :0111-----
:10498 D_K[.8000] ;> FF EXP. OVERFLOW, SET TRAP STACK
:10499 CALL,J/OVFL ;GOTO SET CES FOR OVERFLOW
:10500 =1111
:10501 DEST: :1111-----
:10502 CACHE D[INST.DEP]
:10503 CLR.IB.OPC,PC_PC+1,J/IRD ;WRITE DEST FOR UNDERFLOW, OVERFLOW
:10504
:10505
:10506
:10507 :CLEANUP FOR *** ADDS, RESULT IN D, DEST NOT EVALUATED YET.
:10508 :COME HERE WITH BEN/SC TO TEST FOR UNDERFLOW AND OVERFLOW.
:10509 =0001
:10510 EXPCK: :0001-----
:10511 D 0 ;ZERO EXP. UNDERFLOW, SET TRAP STACK
:10512 CALL,J/UNDRFL ;GOTO SET CES FOR UNDERFLOW
:10513
:10514 WRDST: :0011-----
:10515 WRITE.DEST ;01 TO FF FOR EXP, OK
:10516
:10517 :0101-----
:10518 D 0 ;NEG EXP. UNDERFLOW, SET TRAP STACK
:10519 CALL,J/JNDRFL ;GOTO SET CES FOR UNDERFLOW
:10520
:10521 OVFLK: :0111-----
:10522 D_K[.8000] ;> FF EXP. OVERFLOW, SET TRAP STACK
:10523 CALL,J/OVFL ;GOTO SET CES FOR OVERFLOW
:10524 =1111
:10525 :1111-----
:10526 WRITE.DEST ;WRITE DEST FOR UNDERFLOW, OVERFLOW
  
```

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 L 6 Fiche 2 Frame L6 Sequence 282  
 : P1W124,MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 281  
 : FLOAT .MIC [600,1204] F & D floating point : MULF

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:10527 .TOC   "      F & D floating point : MULF"
:10528
:10529 :MULF, *-R
:10530 :ENTER HERE AT B,FORK WITH LA CONTAINS DST, D CONTAINS SRC.
:10531
:10532 220: -----
:10533 MULF2: Q_D(FRAC)(B),          ;GET SRC FRAC
:10534 SC_D(EXP)(B),                ;GET SRC EXP
:10535 FE_LA(-XP),                 ;GET DST EXP
:10536 SS_ALU15,CHK.FLT.OPR,       ;SS GETS SRC SIGN, CHK -0,
:10537 CLR.UBCC                     ;CLOCK DST EXP
:10538
:10539 -----
:10540 RCE[T0]_Q,FE_SC+FE,          ;PROD EXP = SUM OF EXP'S
:10541 EALU?                      ;DST EXP (EALU.Z), SRC EXP (SC) = 0?
:10542 =01001
:10543 MULF.0: 01001-----
:10544 R(PRN),K[ZERO],SET.CC(INST), ;PROD = 0: SET COND CODES
:10545 CLR.IB,OPC,PC_PC+1,J/IRD   ;
:10546
:10547 01011-----
:10548 D_LA(FRAC),                 ;GET DST FRAC
:10549 LT_RC[T0],Q_0,               ;GET SHIFT VALUE -7
:10550 SC_K[.FFF9],                ;GET RESULTANT SIGN TO SS
:10551 SS_SS.XOR.ALU15&SD_ALU15,  ;
:10552 CALL,J/MULFX               ;
:10553
:10554 ****
:10555 /* Patch no. 088, PCS 006B trapped to WCS 1198 */
:10556 ****
:10557
:10558 01101-----
:10559 ALU_LA,CHK.FLT.OPR,         ;
:10560 J/MULF.0
:10561
:10562 01111-----
:10563 ALU_LA,CHK.FLT.OPR,         ;
:10564 J/MULF.0
:10565
:10566 =11011 11011-----
:10567 ALU?, J/ADDFDX             ;RENORMALIZE (IF NEEDED), PACK & STORE
:10568 =
  
```

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 M 6  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : MULF

Fiche 2 Frame M6

Sequence 283

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```

;10569 ;MULF, *** OR ****
;10570 ;ENTER HERE WITH D CONTAINS DST, Q CONTAINS SRC
;10571 038F:
;10572 MULF: -----
;10573   Q_Q(FRAC)(B),SC_Q(EXP)(B),      ;GET SRC FRAC, EXP
;10574   FE_D(EXP),
;10575   SS_ALU15,CHK.FLT.OPR,CLK.UBCC :
;10576
;10577 -----
;10578   RC[T0] Q,                      ;GET 2 TIMES MULTI'CAND TO LC
;10579   FE_SC+FE,
;10580   EA[U?]
;10581
;10582 =01001 :01001-----
;10583   EALU_K[ZERO],D_K[ZERO],
;10584   SET.CC(INST),
;10585   WRITE.DEST,J/WRD          ;WRITE RESULT FLOAT 0
;10586
;10587 :01011-----
;10588   D_D(FRAC),LC_RC[T0].Q_0,      ;GET DST FRAC
;10589   SC_K[.FFF9],                  ;GET SHIFT VALUE -7
;10590   SS_SS.XOR.ALU15&SD_ALU15,    ;GET RESULTANT SIGN TO SS
;10591   CALL,J/MULFX
;10592
;10593 :01101-----
;10594   ALU_D,CHK.FLT.OPR,D_0,
;10595   J/WR.Z
;10596
;10597 :01111-----
;10598   ALU_D,CHK.FLT.OPR,D_0,
;10599   J/WR.Z
;10600
;10601 =11011 :11011-----
;10602   ALU?, J/ADDFDA          ;RENORMALIZE (IF NEEDED), PACK & STORE
;10603 =

```

22-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 N 6  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 Fiche 2 Frame N6 Sequence 284  
 : FLOAT .MIC [600,1204] F & D floating point : MULF VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 283

```

:10604 ;FRACTION MULTIPLY ROUTINE - USES INTEGER MULTIPLY SUBR
:10605
:10606 ;INPUTS: SC = -7, D = MULTIPLIER FRACTION, SS = RESULT SIGN,
:10607 ; HAS SUM OF INPUT EXPNS, LC HAS 2 * MULTIPLICAND FRACTION,
:10608
:10609 ;OUTPUTS: D = ROUNDED PRODUCT FRACTION,
:10610 ; SC = PRODUCT EXPONENT,
:10611 ; SS & SD = PRODUCT SIGN
:10612
:10613 ;TEMPORARIES: R[R15], LA, LB, Q
:10614
:10615 ;MULFX: -----
:10616 ;D_DAL_SC, R[R15]_LC.RIGHT, SI/ZERO, ;SHIFT M'IER READY, R[R15]_M'CAND
:10617 ;SC_K[.T], SD_SS ;SET LOOP CT FOR 26. BITS
:10618
:10619
:10620 =0* ;0*-----
:10621 ;ALU_0(A), ;LB_M'CAND
:10622 ;D_D.RIGHT2, SI/ZERO, LAB_R[R15], ;CALL.BEN/MUL,J/MULPP ;CALL MULTIPLICATION ROUTINE
:10623
:10624
:10625 ;1*-----
:10626 ;SC_FE, D_Q, Q_D, R[R15]_K[.80] ;ALWAYS POS PROD
:10627
:10628
:10629 ;SC_SC-SHF.VAL, D_DAL.NORM, ;SHIFT LEFT JUSTIFIED
:10630 ;LAB_R[R15]
:10631
:10632
:10633 ;D_D+LB, CLK.UBCC, SC_SC-K[.7C], ;ROUNDING
:10634 ;RETURN10 ;
  
```

U 065D, 0D50,0038,8584,FAF8,0084,6398  
 U 0398, 0203,0C3D,0180,FA78,0000,0350  
 U 039A, 0C18,0038,41E0,FAF8,0081,0664  
 U 0664, 0E00,003C,0180,FA78,008C,A669  
 U 0669, 080D,0016,9D80,F800,0094,A010

8 7

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 Fiche 2 Frame B7 Sequence 285  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 284  
 ; FLOAT .MIC [600,1204] F & D floating point : DIVF

```

:10635 .TOC   "      F & D floating point : DIVF"
:10636
:10637 :DIVF: *--R
:10638 :ENTER HERE AT B.FORK WITH LA CONTAINS DST (D'END), D CONTAINS SRC (D'SOR)
:10639 221:
:10640 DIVF2: -----
:10641     Q_D(FRAC)(B),SC_D(EXP)(B),      ;GET SRC FRACTION
:10642     C[K].UBCC,
:10643     FE_LA(EXP),
:10644     SS_ALU15,CHK.FLT.OPR          ;CK IF NEG FPO
:10645
:10646 -----
:10647     SC_FE,FE_SC,RC[T0]_0,EALU?   ;SWAP EXPS
:10648
:10649 : *****
:10650 : * Patch no. 087, PCS 067E trapped to WCS 1197 *
:10651 : *****
:10652
:10653 =1001 :1001-----
:10654     ALU_LA,CHK.FLT.OPR,J/DIVF6   ;D'SOR = 0: NO DIVIDE
:10655
:10656 :1011-----
:10657     FE_SC-FE,J/DIVF3           ;D'SOR TO LB
:10658
:10659 : *****
:10660 : * Patch no. 022, PCS 058B trapped to WCS 1159 *
:10661 : *****
:10662
:10663 :1101-----
:10664     ALU_LA,CHK.FLT.OPR,J/DIVF6   ;D'SOR = 0: NO DIVIDE
:10665
:10666 :1111-----
:10667     ALU_LA,CHK.FLT.OPR,J/MULF.0 ;D'END = 0
:10668
:10669 =0 DIVF3: :0-----
:10670     D_LA(FRAC),
:10671     SS_SS.XOR.ALU15&SP ALU15.    ;GET D'END FRAC, RESULT SIGN
:10672     LC_RC[T0],CHK.FLT.OPR,
:10673     SC_K[.19],CALL,J/DIVFX       ;D'SOR TO LB, SET LOOP CT FOR 25.
:10674
:10675 :1-----
:10676     ALU?, J/ADDFDX             ;TEST FOR NORM, PACK & STORE
:10677 =0 DIVF6: :0-----
:10678     D_K[.8000],CALL,J/DIVBY0    ;SET CES FOR FL DIV BY 0
:10679
:10680
:10681
:10682 :1-----
:10683     R(PRN)_K[.8000],
:                  CLR.IB.OPC,PC_PC+1,J/IRD
  
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:10684 ;DIVF: ***  

:10685 ;ENTER HERE WITH D CONTAINS DST, Q CONTAINS SRC  

:10686 038D:  

:10687 DIVF: -----  

:10688 Q_Q(FRAC)(B), ;GET SRC FRACTION  

:10689 ST_Q(EXP)(B),CLK,UBCC,  

:10690 FE_D(EXP),SS_ALU15,CHK.FLT.OPR ;CK IF NEG FP0  

:10691  

:10692 -----  

:10693 SC_FE,FE_SC,RC[TO]_Q,EALU? ;SWAP EXPS  

:10694  

:10695 =1001 ;1001-----  

:10696 ALU_D,CHK.FLT.OPR,J/DIVF8 ;D'SOR = 0: NO DIVIDE  

:10697  

:10698 ;1011-----  

:10699 FE_SC-FE,J/DIVF4 ;D'SOR TO LB  

:10700  

:10701 ;*****  

:10702 ; * Patch no. 021, PCS 061B trapped to WCS 1158 *  

:10703 ;*****  

:10704  

:10705 ;1101-----  

:10706 ALU_D,CHK.FLT.OPR,J/DIVF8 ;D'SOR = 0: NO DIVIDE  

:10707  

:10708 ;1111-----  

:10709 ALU_D,CHK.FLT.OPR,D_O, ;D'END = 0, THEREFORE RESULT 0  

:10710 J/WR.Z  

:10711 =0  

:10712 DIVF4: ;0-----  

:10713 D_D(FRAC), ;GET D'END FRAC, RESULT SIGN  

:10714 SS_SS,XOR,ALU15&SD_ALU15,  

:10715 LC_RC[TO],CHK.FLT.OPR, ;D'SOR TO LB, SET LOOP CT FOR 25.  

:10716 SC_K[.19],CALL,J/DIVFX  

:10717  

:10718 ;1-----  

:10719 ALU?, J/ADDFDA ;TEST FOR NORM, PACK & STORE
  
```

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1WI24.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : DIVF

D 7

Fiche 2 Frame D7

Sequence 287

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;10720 : FRACTION DIVIDE ROUTINE - RESTORING METHOD. ENTER AT DIVFX  
 ;10721  
 ;10722 : INPUTS: D = DIVIDEND FRACTION  
 ;10723 LC = RC[T0] = DIVISOR FRACTION  
 ;10724 SS = QUOTIENT SIGN  
 ;10725 SC = 19 (HEX)  
 ;10726 FE = DIFFERENCE IN INPUT EXPONENTS  
 ;10727 Q<6:0> = 0  
 ;10728  
 ;10729 : OUTPUTS: D = ROUNDED QUOTIENT FRACTION  
 ;10730 SS = SD = QUOTIENT SIGN  
 ;10731 SC = BIASED QUOTIENT EXPONENT  
 ;10732  
 ;10733 : TEMPORARIES: R[R15], LA, LB, Q  
 ;10734  
 ;10735 =011  
 ;10736 DIVFO: :011-----  
 ;10737 R[R15] K[.80]. ;SET UP FOR PACK FP  
 ;10738 D\_Q,Q\_0,SC\_SC+FE,SD\_SS,  
 ;10739 J7DIVF1 ;SC HAS -1 (SHOULD HAVE  
 ;10740 ;K[.87] IN NEXT STATE)  
 ;10741  
 ;10742 DIVFX: :111-----  
 ;10743 ALU D-LC.  
 ;10744 DK/DIV, Q\_Q.LEFT,  
 ;10745 SHF/LEFT,S/DIV,  
 ;10746 SC\_SC-K[.1].MUL? J/DIVFO ;LOOP FOR DIV  
 ;10747  
 ;10748 DIVF1: -----  
 ;10749 SC\_SC-SHF.VAL,D\_DAL.NORM.  
 ;10750 LAB\_R[R15] ;NORMALIZE FIRST  
 ;10751  
 ;10752 ;-----  
 ;10753 D\_D+LB,CLK.USCC,SC\_SC+K[.88]. ;ROUNDING, AND ADD 80 TO ADJUST EXP  
 ;10754 RETURN1  
 ;10755 =0  
 ;10756 DIV'8: :0-----  
 ;10757 D\_K[.8000].CALL,J/DIVBY0 ;SET CES FOR FL DIV BY 0  
 ;10758  
 ;10759 ;1-----  
 ;10760 WRITE.DEST,J/WRD ;

U 0323, 0C18,0038,41FC,FAF8,0080,8694  
 U 0327, 0431,0C00,06A8,F800,0084,A323  
 U 0694, 0E00,003C,0180,FA78,008C,A6A6  
 U 06A6, 080D,0016,C580,F800,0094,8001  
 U 03E0, 0818,0039,4580,F800,0000,0E00  
 U 03E1, F000,003F,01F0,F847,0000,0300

E 7

Fiche 2 Frame E7      Sequence 288  
VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124      Page 287

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204]      F & D floating point 14-Jan-82  
 : P1W124.MCR 600,1204]      MICRO2 1L(03)      14-Jan-82 15:30:16  
 ; FLOAT .MIC [600,1204]      F & D floating point : CMPD

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:10761 .TOC   "      F & D floating point : CMPD"
:10762
:10763 :DOUBLE PRECISION FLOATING POINT CMP.
:10764 :ENTER HERE WITH SRC<H,L> = RC[T0], Q; DST<H,L> = RC[T1], D.
:10765
:10766 :ALGORITHM:
:10767 :SIMILAR TO CMPF, WITH THE FOLLOWING SET OF TESTS BEING USED
:10768 :FOR MAGNITUDE COMPARISON:
:10769 :1. EXPONENTS
:10770 :2. FRACTION<0:23> (BIT 0 IS MOST SIGNIFICANT IN THIS NOTATION)
:10771 :3. FRACTION<24:39>
:10772 :4. FRACTION<40:55>
:10773
:10774 :*** NOTE ***
:10775 :THIS ROUTINE HAS A MAJOR BUG, STARTING AT THE MICROINSTRUCTION
:10776 :AFTER THE ONE LABELLED 'GETL1' AND CONTINUING TO THE END OF THE
:10777 :INSTRUCTION. SEE THE ECO LISTING FOR CORRECTIONS.
:10778
:10779 382:
:10780 :-----: CMPD: ID[T1]_D, D_Q, ALU_RC[T1], ;SAVE DST<L>, GET DST<H>
:10781 :-----: SC_ALU(EXP), Q_ALU(FRAC), ;UNPACK DST<H>
:10782 :-----: SS_ALU15, CHK.FLT.OPR ;AND CHECK FOR -0
:10783
:10784 :-----: ID[T2]_D, ALU_RC[T0], FE_SC, ;SAVE SRC<L>, GET SRC<H>
:10785 :-----: D_ALU(FRAC),
:10786 :-----: ST_ALU(EXP), CLK.UBCC, ;UNPACK SRC<H>, SET CC ON EXPS
:10787 :-----: SS_SS_XOR_ALU15&SD_ALU15, ;SS=0 IF SIGNS EQUAL
:10788 :-----: CHR.FLT.OPR, SC.GT.0? ;TEST FOR -0 SRC & 0 DST
:10789
:10790 ==01
:10791 :-----: ALU_RC[T0].SET.CC(INST),
:10792 :-----: CLR_IB.OPC,PC_PC+1, ;DST = 0, CC SET BY SRC
:10793 :-----: J/IRD
:10794
:10795 :-----: ALU_D-Q_EALU_SC-FE_CLK.UBCC, ;SRC - DST FOR FRAC, EXPS
:10796 :-----: Q_ID[T1], LC_RC[T1], ;GET DST<L> IN Q, SRC<H> IN LC
:10797 :-----: EALU? ;BEN ON SS - EALU NZ KNOWN 0
:10798
:10799 ==10
:10800 :-----: R[R15]_LC, D_Q, Q_ID[T2], ;R[R15]_DST<H>, D=DST<L>, Q=SRC<L>
:10801 :-----: EALU?,J/GETLT ;COMPARE SRC - DST EXPS
:10802
:10803 :-----: R[R15]_LC, J/CHECKF ;SGNS DIFF - SET CC'S FROM -DST
:10804 :-----: ;(CANT SET FROM SRC, MAY BE 0)
:10805
:10806 ==011
:10807 :-----: GETL1: ALU_RC[T0].SET.CC(INST),
:10808 :-----: CLR_IB.OPC,PC_PC+1,J/IRD ;SRC(EXP) > DST(EXP), CC_SRC
:10809
:10810 :-----: ALU_Q-D, WORD, ALU?, J/CHECKH ;CHECK SRC - DST FRAC<H>'S **SEE ECO**
:10811
:10812 :-----: * Patch no. 008, PCS 0627 trapped to WCS 1148 *
:10813
:10814 :-----: ****

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:10815 -----;
:10816 ALU_R[R15].XOR.K[.8000], ;DST(EXP) > SRC(EXP), CC_-DST
:10817 SET.CC(INST),
:10818 CLR.IB.OPC,PC_PC+1,J/IRD
:10819 =;END ;-----;
:10820
:10821 =0011
:10822 CHECKH: ALU_RC[T0],SET.CC(INST), ;SRC<H> > DST<H>, CC_SRC
:10823 CLR.IB.OPC,PC_PC+1,
:10824 J/IRD
:10825 ;-----;
:10826 ALU_Q-D, LONG, ALU?, J/CHECKL ;SRC<H>=DST<H> - TEST SRC<M>-DST<M>
:10827 -----;
:10828 ALU_R[R15].XOR.K[.8000], ;DST<H> > SRC<H>, CC_-DST
:10829 SET.CC(INST),
:10830 CLR.IB.OPC,PC_PC+1,J/IRD
:10831 =;END ;-----;
:10832
:10833 =0011
:10834 CHECKL: ALU_RC[T0],SET.CC(INST), ;SRC<M> > DST<M>, CC_SRC
:10835 CLR.IB.OPC,PC_PC+1,
:10836 J/IRD
:10837 ;-----;
:10838 ALU?, J/CHECKF ;SRC<M>=DST<M> - TEST SRC<L>-DST<L>
:10839 ;-----;
:10840 ALU_R[R15].XOR.K[.8000], ;DST<M> > SRC<M>, CC_-DST
:10841 SET.CC(INST),
:10842 CLR.IB.OPC,PC_PC+1,J/IRD
:10843 =;END ;-----;
:10844
:10845 =1010
:10846 CHECKF: ALU_R[R15].XOR.K[.8000], ;DST<L> > SRC<L>, CC_-DST
:10847 SET.CC(INST),
:10848 CLR.IB.OPC,PC_PC+1,J/IRD ;UPDATE PC, POP IB FOR NXT INST
:10849 ;-----;
:10850 ALU_RC[T0],SET.CC(INST), ;SRC<L> > DST<L>, SRC SET CC
:10851 CLR.IB.OPC,PC_PC+1,J/IRD
:10852 ;-----;
:10853 =1111 ALU_K[ZERO],SET.CC(INST), ;SRC<L> = DST<L>
:10854 CLR.IB.OPC,PC_PC+1,J/IRD ;UPDATE PC, POP IB, GOTO NXT INST
:10855 ;-----;

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ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204]  
; P1W124.MCR 600,1204]  
; FLOAT .MIC [600,1204]

F & D floating point  
MICRO2 1L(03) 14-Jan-82 14-Jan-82 15:30:16  
F & D floating point : UNPACK DOUBLE OPERANDS

G 7

Fiche 2 Frame G7

Sequence 290

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;10856 .TOC " F & D floating point : UNPACK DOUBLE OPERANDS"  
;10857  
;10858 :ROUTINE TO UNPACK DOUBLE FLOATING POINT OPERANDS.  
;10859 :INPUTS: RC[T0] = OPERAND 1 HIGH LONGWORD  
;10860 : Q = RC[T3] = OPERAND 1 LOW LONGWORD  
;10861 : D = OPERAND 1 LOW LONGWORD, WITH HIGH AND LOW WORD SWAPPED  
;10862 : RC[T1] = OPERAND 2 HIGH LONGWORD  
;10863 : RC[T6] = OPERAND 2 LOW LONGWORD  
;10864 : SC = -7  
;10865 : IR<2:1> = TYPE OF OPERATION BEING PERFORMED:  
;10866 : 00 = ADD, 01 = SUB, 10 = MUL, 11 = DIV  
;10867  
;10868 : (STARTING WITH THE OPERANDS IN <RC[T0],Q> AND <RC[T1],D>,  
;10869 : THE FOLLOWING SEQUENCE OF STATES SETS THINGS UP RIGHT:  
;10870 : RC6\_D, D\_Q, SC\_16.  
;10871 :=00 2: D\_DL\_SC, RC3\_D, SC\_-7, CALL UNPACK )  
;10872  
;10873 :OUTPUTS:  
;10874 : ID[T0] = OPERAND 1 FRACTION <H>  
;10875 : Q = ID[T2] = OPERAND 1 FRACTION <L>  
;10876 : RC[T5] = ID[T1] = OPERAND 2 FRACTION <H>  
;10877 : D = OPERAND 2 FRACTION <L>  
;10878 : SC = OPERAND 2 EXPONENT  
;10879 : FE = NARS(EXPONENT DIFFERENCE) IF IR<2:1> = 00 OR 01,  
;10880 : = SUM OF EXPONENTS IF IR<2:1> = 10,  
;10881 : = (EXPONENT OF OPERAND 1) - (EXPONENT OF OPERAND 2) IF IR<2:1>=11  
;10882 : SS = (SIGN OF OPERAND 1) .XOR. (SIGN OF OPERAND 2) .XOR. IR<1>  
;10883 : RC[T0], RC[T1], RC[T3], RC[T6] PRESERVED  
;10884  
;10885 :TEMPORARIES: ID[T3] HOLDS OPERAND 1 <L>,  
;10886 : RER15J HOLDS OPERAND 1 <H>,  
;10887 : LA, LB, LC HOLD VARIOUS THINGS  
;10888  
;10889 :RETURNS: RETURN @ 1 IF OPERAND 1 = 0  
;10890 : RETURN @ 2 IF OPERAND 1 <> 0, OPERAND 2 = 0  
;10891 : RETURN @ 3 IF BOTH OPERANDS ARE NON-ZERO  
;10892  
;10893 :UNPACK: -----  
;10894 : LC\_RC[T0], : LATCH SRC0 <H>  
;10895 : FE\_K[.7] : SETUP SHIFT AMOUNT FOR UNPACK FRAC <H>  
;10896  
;10897 :-----  
;10898 : ID[T3] D, : SAVE SRC IMMED <L>  
;10899 : D\_LC(FRAC), : UNPACK SRC0 <H>  
;10900 : \_0, : SETUP FOR FRAC <H>  
;10901 : SS\_ALU15, : SS GETS SRC SIGN  
;10902 : CHR.FLT.OPR, : CHK RSV OPD  
;10903 : SET.CC(INST) : SET COND CODES IN CASE DEPEND SOLELY ON SRC  
;10904  
;10905  
;10906 : D\_DL\_SC, SD\_SS, : SHIFT RIGHT BY 7, SAVE SS IN SD  
;10907 : Q\_ID[T3], : GET SRC IMMED <L>  
;10908 : SC\_FE, : SC GETS 7  
;10909 : RER15J\_LC : SAVE SRC0 <H>

U 06CA, 0000,003C,5D80,F900,0104,66CE

U 06CE, 0910,C038,CDF9,3C00,0870,0720

U 0720, 0D10,0038,CDF4,2EF8,0081,0731

ZZ-ESOAA-124.0 ; FLOAT .MIC [600.1204] F & D floating point 14-Jan-82  
 : P1W124.MCR 600.1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600.1204] F & D floating point : UNPACK DOUBLE OPERANDS

H 7

Fiche 2 Frame H7

Sequence 291

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U 0731. 0D18.0038.1981.FA78.0118.5736

:10910 :-----;  
 :10911 D\_DAL.SC, ALU\_K[ZERO], : GET SRC FRAC <H>  
 :10912 FE\_R[15](EXP), : FE GETS SRC EXP  
 :10913 CLR.UBCC, SS\_ALU15 : SET BRANCH COND CODE FOR SRC EXP, CLR SS  
 :10914  
 :10915 :-----;  
 :10916 ID[T0]\_D, : SAVE SRC FRAC <H>  
 :10917 LC\_RC[T1], SS\_SD, : LATCH DSTO <H>, RESTORE SS TO OLD VALUE  
 :10918 D\_Q, Q\_O, : SETUP FOR SHIFTING SRC FRAC <L>  
 :10919 EALU.Z? : IS SRC EXP = 0 ? (\*\*NOTE SS IS CLEAR!)  
 :10920

:10921 =\*01\* :0-----; NO: SRC\_NE\_0 (EALU => 0) (SS=0)  
 :10922 SC\_LC(EXP), : SC GETS DST EXP  
 :10923 SGN/ADD.SUB, : SS GETS FLAG OF +/- FOR ADDD, SUBD  
 :10924 : AND RESULT SIGN FOR MULD, -SIGN FOR DIVD  
 :10925  
 :10926 CHKFLT.OPR, : SD GETS DST SIGN  
 :10927 D\_DAL.SC, : CK IF RSV OPD  
 :10928 FE\_K[10], : D GETS SRC FRAC <L>  
 :10929 IR2-1?,J/SRCL : SETUP SHIFT AMOUNT  
 :10930  
 :10931 :1-----; GOTO SAVE SRC FRAC <L> AND CK FOR +, -, \*, /

U 02DA. 0D10.0938.6586.F800.0987.64D8

:10932 D\_LC, : YES: SRC = 0  
 :10933 SC\_LC(EXP), : D GETS DSTO <H>  
 :10934 CHRFLT.OPR, : SC GETS DST EXP  
 :10935 SET.CC(INST) : CK IF RSV OPD  
 :10936 =:END : SET COND CODES

U 02DE. 0810.C038.0180.F800.08F3.073D

:10937 :-----;  
 :10938 Q\_RC[T6], : GET DSTO <L>  
 :10939 SC\_GT.0? : DST EXP = 0?

U 073D. 0010.1438.01C0.F930.0000.0361

:10940 :-----;  
 :10941 =\*01 :0-----; SRC = 0, DST = 0  
 :10942 RC[T1]\_K[ZERO], : RESULT IS 0  
 :10943 D\_Q, Q\_O, : RETURN ADR .OR. 1 FOR SRC = DST = 0  
 :10944 RETURNT

U 0361. 0F18.003A.19F8.F988.0000.0001

:10945 :-----;  
 :10946 :1-----; SRC = 0, DST\_NE\_0  
 :10947 RC[T1]\_Q, : RC1 GETS DSTO <L>  
 :10948 Q\_O, : CLR Q  
 :10949 RETURN1 : RETURN ADR .OR. 1 FOR SRC = 0, DST\_NE\_0

U 0363. 0001.203E.01F8.F988.0000.0001

=:END

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : UNPACK DOUBLE OPERANDS

I 7

Fiche 2 Frame I7

Sequence 292

Page 291

U 04D8, 0810,1438,C9C0,3D30,0199,E371

:10951	=00		
:10952	SRCL:	:00-----	ADDD
:10953		FE_NABS(SC-LA(EXP)),	FE GETS NABS(DST(EXP) - SRC(EXP))
:10954		SC_FE,	SC GETS 16.
:10955		CLR.UBCC,	SET BRANCH COND CODES
:10956		ID[T2] D,	SAVE UNPACKED SRC FRAC <L>
:10957		D_RC[T6], Q_RC[T6],	GET DSTO <L> FOR SWAP WORD
:10958		SC.GT.0?,J/BSTTST	DST EXP = 0?
:10959			
:10960		:01-----	SUBD
:10961		FE_NABS(SC-LA(EXP)),	FE GETS NABS(DST(EXP) - SRC(EXP))
:10962		SC_FE,	SC GETS 16.
:10963		CLR.UBCC,	SET BRANCH COND CODES
:10964		ID[T2] D,	SAVE UNPACKED SRC FRAC <L>
:10965		D_RC[T6], Q_RC[T6],	GET DSTO <L> FOR SWAP WORD
:10966		SC.GT.0?,J/BSTTST	DST EXP = 0?
:10967			
:10968		:10-----	MULD
:10969		FE_SC+LA(EXP),	FE GETS DST(EXP) + SRC(EXP)
:10970		SC_FE,	SC GETS 16.
:10971		CLR.UBCC,	SET BRANCH COND CODES
:10972		ID[T2] D,	SAVE UNPACKED SRC FRAC <L>
:10973		D_RC[T6], Q_RC[T6],	GET DSTO <L> FOR SWAP WORD
:10974		SC.GT.0?,J/BSTTST	DST EXP = 0?
:10975			
:10976		:11-----	DIVD
:10977		FE_SC-LA(EXP),	FE GETS (DST(EXP) - SRC(EXP))
:10978		SC_FE,	SC GETS 16.
:10979		CLR.UBCC,	SET BRANCH COND CODES
:10980		ID[T2] D,	SAVE UNPACKED SRC FRAC <L>
:10981		D_RC[T6], Q_RC[T6],	GET DSTO <L> FOR SWAP WORD
:10982		SC.GT.0?	DST EXP = 0?
:10983	=END		

U 04DA, 0810,1438,C9C0,3D30,0199,8371

U 04DB, 0810,1438,C9C0,3D30,0199,A371

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 J 7  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCST24 Sequence 293  
 : FLOAT .MIC [600,1204] F & D floating point : UNPACK DOUBLE OPERANDS Page 292

	:10984	=*01	
	:10985	DSTTST: ;0-----	
	:10986	D_LA,	DST = 0, SRC.NE.0, D GETS SRC0 <H>
	:10987	LTCRC[T3],	LATCH SRC0 <L>
	:10988	RETURN2	RETURN ADR.OR.2 FOR DST = 0, SRC.NE.0
	:10989		
	:10990	:1-----	DST.NE.0, SRC.NE.0
	:10991	D_DAL.SC,	SWAP WORD DST FRAC <L>
	:10992	Q_RCT1](FRAC),	UNPACK DST0 <H>
	:10993	SC_K[.19]	SHIFT AMOUNT SET TO 25.
	:10994	=;END	
	:10995		
	:10996	D_DAL.SC,	SHIFT DST FRAC
	:10997	Q_D	GET FRAC LOWER PART
	:10998	SC_K[.7]	SHIFT AMOUNT SET TO 7
	:10999		
	:11000		
	:11001	D_DAL.SC	GET DST FRAC <H>
	:11002		
	:11003		
	:11004	ID[T1]_D, RC[T5]_D.	SAVE DST FRAC <H>
	:11005	D_Q, Q_O	SETUP FOR FRAC <L>
	:11006		
	:11007		
	:11008	D_DAL.SC,	D GETS DST FRAC <L>
	:11009	Q_ID[T2],	Q GETS SRC FRAC <L>
	:11010	ST_RCT1](EXP),	SC GETS DST EXP
	:11011	RETURN3	RETURN ADR.OR.3 FOR DST.NE.0, SRC.NE.0

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 Fiche 2 Frame K7 Sequence 294  
 : P1WT24.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 293  
 : FLOAT .MIC [600,1204] F & D floating point : PACK DOUBLE RESULT

K 7

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:11012 .TOC   "      F & D floating point : PACK DOUBLE RESULT"
:11013
:11014 :ROUTINE TO PACK DOUBLE FLOATING POINT RESULT.
:11015 :ENTRY:      AT 'PACKD'
:11016 :INPUTS:     D = NORMALIZED FRACTION<H>, UNROUNDED
:11017 :           Q = NORMALIZED FRACTION<L>, ROUNDED
:11018 :           C31 = CARRY FROM ROUNDING Q
:11019 :           SC = BIASED EXPONENT
:11020 :           SD = SIGN
:11021 :           FE = 18 (HEX)
:11022 :           STATE<0> = 1 IF CALLED FROM POLYD, ELSE 0
:11023 :           STATE<3:1> = 0
:11024 :OUTPUTS: (IF NOT CALLED FROM POLYD)
:11025 :           D = RESULT<H>
:11026 :           Q = RC[T1] = RESULT<L>
:11027 :           CONDITION CODES SET
:11028 :           TRAP CODE SET IN ID[CES] IF UNDERFLOW OR OVERFLOW OCCURRED
:11029 :OUTPUTS: (IF CALLED FROM POLYD)
:11030 :           Q = RC[T1] = RESULT<H>
:11031 :           D = RESULT<L>
:11032 :           SC = FE = EXPONENT
:11033 :TEMPORARIES: LC
:11034 :RETURNS:      RETURNS @ 10 IF NOT CALLED FROM POLYD
:11035 :           RETURNS @ 10 IF CALLED FROM POLYD AND EXPONENT = 0
:11036 :           RETURNS @ 12 OR 13 IF CALLED FROM POLYD AND 1 < EXPONENT < 100
:11037 :           RETURNS @ 15 IF CALLED FROM POLYD AND EXPONENT < 0
:11038 :           RETURNS @ 17 IF CALLED FROM POLYD AND EXPONENT > FF
:11039 :
:11040 :=0*
:11041 :PACKD.0: ;0-----
:11042 :           D_DAL.SC, SC_FE,
:11043 :           EALU_K[.1], CLK.LBCC, : D GETS FRAC <L>, SC GETS BACK EXP
:11044 :           STATE0?, J/PACKD.2 : CLEAR EALU CC'S
:11045 :           ;-----: CHECK FOR POLYD AND GO SWAP FRAC<L>
:11046 :           1-----:
:11047 :           D_D+K[.1],
:11048 :           SC_FE, FE_SC, : FRAC <H> INCREMENTED BY 1
:11049 :           CLR.LBCC : SC GETS EXP, FE GETS 24.
:11050 :           ;-----: CLOCK IN CARRY IF ANY
:11051 :;END
:11052 :           ALU_0+K[.1],CLK.LBCC, : CLR C31
:11053 :           C31? : HAVE TO INCREMENT EXP BY 1?
:11054 :=0*
:11055 :PACKD: ;0-----
:11056 :           SC_FE, FE_SC, : NO, PACK RESULT <H>
:11057 :           RC[T1] PACK.FP, : SC GETS 24, AND FE SAVES EXP
:11058 :           SET_CC(INST), : RC1 GETS PACKED RESULT <H>
:11059 :           C31? : SET COND CODES
:11060 :           J/PACKD.0 : HAVE TO INCREMENT FRAC <H>?
:11061 :           ;-----: GOTO PACK FRAC <L> OR INCREMENT FRAC <H>
:11062 :           1-----: YES, INCREMENT EXP BY 1
:11063 :           SC_SC+1,J/PACKD : ;-----:
:11064 :;END
  
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U 03EC, 0D00,173C,0580,F800,0095,63E4  
 U 03EE, 0819,0014,0580,F800,0191,0768  
 U 0768, 001B,0314,0580,F800,0010,03FC  
 U 03FC, 0008,C338,0180,F988,01F1,03EC  
 U 03FE, 0000,003C,0180,F800,0080,C3FC

U 03E4, 0018,1438,65E0,F800,0182,0661

:11065 =\*\*+0  
 :11066 PACKD.2: :0-----  
 :11067 SC\_K[.10].ALU.  
 :11068 FE\_SC,  
 :11069 Q\_D,  
 :11070 SC?,J/PACKD.4  
 :11071 :1-----  
 :11072 SC\_K[.10].ALU.  
 :11073 FE\_SC,  
 :11074 Q\_D,  
 :11075 J7PACKD.8

NOT POLYD  
 SC GETS 16, FOR WORD SWAP FOR FRAC <L>  
 SAVE EXP FOR SETTING COND CODES LATTER  
 READY FOR SWAP WORD FOR FRAC <L>  
 EXP SHOWS 0, NON-0, UNDERFLOW, OVERFLOW

U 03E5, 0018,0038,65E0,F800,0182,0775

:11077 =;END  
 :11078 =0001  
 :11079 PACKD.4: :00-----  
 :11080 D\_0,Q\_0,EALU\_K[ZERO],  
 :11081 RC[T1] K[ZERO],  
 :11082 SET\_CC(INST),  
 :11083 CALL,J/UNDRFL

0 EXP: RESULT UNDERFLOW  
 SET RESULT <H,L> TO ZEROS  
 RESULT <L> SET TO 0  
 SET COND CODES  
 SET CES FOR UNDERFLOW

U 0661, 0F18,C039,19F8,F988,0074,6E09

:11084 :01-----  
 :11085 D\_DAL\_SC.  
 :11086 Q\_RC[T1],  
 :11087 J7PACKD.6

01 TO FF EXP: OK  
 SWAP WORD  
 Q GETS RESULT <H>

U 0663, 0D10,0038,01C0,F908,0000,0771

:11088 :10-----  
 :11089 D\_0,Q\_0,EALU\_K[ZERO],  
 :11090 RC[T1] K[ZERO],  
 :11091 SET\_CC(INST),  
 :11092 CALL,J/UNDRFL

NEG EXP: UNDERFLOW  
 SET RESULT <H,L> TO ZEROS  
 RESULT <L> SET TO 0  
 SET COND CODES  
 SET CES FOR UNDERFLOW

U 0665, 0F18,C039,19F8,F988,0074,6E09

:11093 :11-----  
 :11094 D\_K[.8000],  
 :11095 SET\_CC(INST),  
 :11096 CALL,J/OVFL

> 31 EXP: OVERFLOW  
 PASS EXP FOR COND CODES DETECTION  
 RESULT SET TO -0  
 SET COND CODES  
 SET CES FOR OVERFLOW

U 0667, 0818,C039,4580,F800,0070,6E03

:11097 EALU\_FE,  
 :11098 D\_K[.8000],  
 :11099 SET\_CC(INST),  
 :11100 CALL,J/OVFL

RETURN FROM CES SETTING  
 RESULT <L> SET TO 0  
 RETURN TO INSTR CALLED FROM FORK ENTRIES

U 066f, 0018,003A,19F8,F988,0000,0010

:11101 :1111 :-----  
 :11102 RC[T1] K[ZERO],Q\_0,  
 :11103 RETURN0  
 :11104 =;END

RETURN FROM CES SETTING  
 RESULT <L> SET TO 0  
 RETURN TO INSTR CALLED FROM FORK ENTRIES

U 0771, 0C01,003E,01E0,F988,0000,0010

:11105 :1116 :-----  
 :11106 D\_Q,  
 :11107 RETURN10  
 :11108 RC[T1]\_D, Q\_D,  
 :11109 D\_Q,  
 :11110 RETURN10

RC1, Q HAVE RESULT <L>  
 D GETS RESULT <H>  
 RETURN TO INSTR CALLED FROM FORK ENTRIES

U 0775, 0D10,0038,01C0,F908,0081,0776

:11111 :11112 :-----  
 :11112 D\_DAL\_SC,SC\_FE,  
 :11113 Q\_RC[T1]  
 :11114 =;END  
 :11115 SC?,RETURN10

POLYD  
 SWAP WORD, GET BACK EXP  
 Q GETS RESULT <H>

U 0776, 0000,143E,0180,F800,0000,0010

1

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 Fiche 2 Frame M7 Sequence 296  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 295  
 : FLOAT .MIC [600,1204] F & D floating point : ADDD, SUBD

U 0042, 0001,203C,19F8,F980,1404,6778	:11118 .TOC " F & D floating point : ADDD, SUBD"
L 0778, 0000,003C,0180,F988,0000,077B	:11119 :ADDD2/SUBD2, SHORT LITERAL (SL) - REGISTER (R)
U 0778, 0800,003C,0180,F870,0000,0225	:11120 ;ENTER HERE FROM IRD STATE AT A.FORK WITH SL IN Q, R IN LA.
U 0225, 0C01,003D,6580,F980,0084,6580	:11121 :11122 :11123 042: :----- :11124 STATE K[ZERO], : CLR POLYD FLAG :11125 RC[T0]_Q, Q_0 : SRC0 <RC0, Q> GETS <SL, R> :11126 :11127 :----- :11128 RC[T1]_LA : RC1 GETS DSTO <H> :11129 :11130 ADDD.A: :----- :11131 D_R(SP1+1) : D GETS DSTO <L> :11132 :11133 =0**** ADDD.R: :0----- :11134 RC[T6]_D, : SAVE DSTO <L> :11135 D_Q, : D GETS SRC0 <L> :11136 SC_K[.10], : SC GETS 16. FOR SWAP WORD OF FRAC <L> :11137 CALL,J/ADDD.S : CALL ADDD/SUBD SUBROUTINE :11138 :11139 :11140 :----- :11141 R(SP1)_D : RETURN WITH RESULT IN <D, RC1> :11142 :----- :11143 =;END : STORE RESULT <H> :11144 :11145 :LC_RC[T1] : GET RESULT <L> :11146 :11147 :11148 :----- :11149 R(SP1+1)_LC, : STORE RESULT <L> :11150 CLR_IB0-T,PC_PC+2, : CLR IB BYTES 0,1 :11151 J/IRD : GOTO NEXT INST :11152 :11153 :ADDD2/SUBD2, R-R :11154 ;ENTER HERE FROM IRD STATE AT A.FORK WITH LB, LA HAVE SRC <H>, DST<H> :11155 :11156 046: :----- :11157 STATE K[ZERO], : CLR POLYD FLAG :11158 RC[T0]_LB : RC0 GETS SRC0 <H> :11159 :11160 :----- :11161 RC[T1]_LA : RC1 GETS DSTO <H> :11162 :11163 :11164 :----- :11165 Q_R(PRN+1), : Q GETS SRC0 <L> :11166 J7ADDD.A : GOTO SAME FLOW AS SI-R

N 7

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 Fiche 2 Frame N7 Sequence 297  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 296  
 : FLOAT .MIC [600,1204] F & D floating point : ADDD, SUBD

U 0242, 0F01,203C,19E0,F988,1404,6225

:11166 :ADDD3/SUBD3, \*-SL-R  
 :11167 :ENTER HERE AT B-FORK WITH SRC0 IN <RC0, D>, SL IN Q.  
 :11168 :LEAVE HERE WITH SRC0 IN <RC0, Q>, DSTO IN <RC1, D>  
 :11169  
 :11170 242: :-----  
 :11171 STATE\_K[ZERO], : CLR POLYD FLAG  
 :11172 RC[T1]\_Q, : RC1 GETS DSTO <H>  
 :11173 Q\_D, D\_O, : Q GETS SRC0 <L>, D GETS DSTO <L> WHICH IS 0  
 :11174 J7ADDD.R  
 :11175  
 :11176 :ADDD3/SUB3, \*-R-R  
 :11177  
 :11178 246: :-----  
 :11179 STATE\_K[ZERO], : CLR POLYD FLAG  
 :11180 RC[T1]\_LA, : RC1 GETS DSTO <H>  
 :11181 Q\_D : Q GETS SRC0 <L>  
 :11182  
 :11183  
 :11184 D\_R(PRN+1), : GET DSTO <L>  
 :11185 J7ADDD.R  
 :11186  
 :11187 :ADDD2/SUBD2, \*-R  
 :11188 :ENTER HERE AT B-FORK WITH SRC0 IN <RC0, D>, R IN LA, LB.  
 :11189 :LEAVE HERE WITH SRC0 IN <RC0, Q>, DSTO IN <RC1, D> TO GOTO SAME FLOW  
 :11190 :AS SL-R, R-R.  
 :11191  
 :11192 22E: :-----  
 :11193 STATE\_X[ZERO], : CLR POLYD FLAG  
 :11194 RC[T1]\_LA, : RC1 GETS DSTO <H>  
 :11195 Q\_D : Q GETS DSTO <L>  
 :11196  
 :11197  
 :11198 D\_R(PRN+1) : D GETS DSTO <L>  
 :11199  
 :11200 =0110\* :00 :-----  
 :11201 RC[T6]\_D, : SAVE DSTO <L>  
 :11202 D\_Q : D GETS SRC0 <L>  
 :11203 SC\_K[.10], : SC GETS 16. FOR SWAP WORD OF FRAC <L>  
 :11204 CALL.J/ADDD.S : CALL ADDD/SUBD SUBROUTINE  
 :11205  
 :11206 =1110\* ADDD.M: :10 :-----  
 :11207 R(PRN)\_D,J/ADDD.P : RETURN WITH RESULT IN <D, RC1>  
 :11208 :----- STORE RESULT <H>  
 :11209  
 :11210 :11 :-----  
 :11211 R(PRN)\_D,SET.V : RETURN WITH RESULT IN <D, RC1>  
 :11212 :----- RESET PSL<V> FOR DIVD  
 :11213  
 :11214 ADDD.P: :-----  
 :11215 LC\_RC[T1] : GET RESULT <L>  
 :11216  
 :11217  
 :11218 R(PRN+1)\_LC :-----  
 :11219 CLR.IB.OPC,PC\_PC+1, : SICRE RESULT <L>  
 :11220 J/\_RD : CLR IB BYTE 0  
 :----- GOTO NEXT INST

U 022E, 0000,003C,19E0,F988,1404,6791

U 0791, 0800,003C,0180,F860,0000,00EC

U 00EC, 0C01,003D,6580,F980,0084,6580

U 00FC, 0001,003C,0180,F8D8,0000,0796

U 00FE, 0001,003C,0180,F8D8,0020,0796

U 0796, 0000,003C,0180,F908,0000,079A

U 079A, C010,0038,0180,F8E4,4000,0062

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
; FLOAT .MIC [600,1204] F & D floating point : ADDD, SUBD

B 8

Fiche 2 Frame B8

Sequence 298

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:11221 :DOUBLE FLOATING POINT ADDD AND SUBD \*\*\* OR \*\*\*  
:11222 :ENTER AT C.FORK WITH SRC OPD IN <RC0, Q>, DST OPD IN <RC1, D>.  
:11223 :ALWAYS YIELDS NORMALIZED AND ROUNDED RESULT.  
:11224  
:11225 38A:  
:11226 ADDD: -----;  
:11227 STATE\_K[ZERO] : CLR POLYD FLAG  
:11228  
:11229 =0\*\*\*\* :0-----;  
:11230 RC[T6]\_D. : SAVE DSTO <L>  
:11231 D\_Q. : D GETS SRC0 <L>  
:11232 SC\_K[.10]. : SC GETS 16. FOR SWAP WORD OF FRAC <L>  
:11233 CALL\_J/ADDD.S : CALL ADDD/SUBD SUBRT  
:11234  
:11235 :1-----;  
:11236 WRITE\_DEST,J/WRD : WRITE RESULT  
:11237 =;END

U 038A, 0000,003C,1980,F800,1404,62A4

U 02A4, 0C01,003D,6580,F980,0084,6580

U 02B4, F000,003F,01F0,F847,0000,0300

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 ; FLOAT .MIC [600,1204] F & D floating point : ADDD, SUBD

C 8

Fiche 2 Frame C8

Sequence 299

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:11238 ; COMMON DOUBLE FLOATING ADD/SUB ROUTINE
:11239
:11240 :INPUTS:      RC[T0] = SRC<H>
:11241 :           D = Q = SRC<L>
:11242 :           RC[T1] = DST<H>
:11243 :           RC[T6] = DST<L>
:11244 :           SC = 10 (HEX)
:11245 :           STATE = 0
:11246 :           IR<1> = 0 IF ADDD, 1 IF SUBD
:11247
:11248 :OUTPUTS:      D = PACKED ROUNDED SUM<H>
:11249 :           RC[T1] = PACKED ROUNDED SUM<L>
:11250 :           CONDITION CODES AND ID[CES] SET ON SUM
:11251
:11252 :TEMPORARIES:   R[R15], RC[T2], RC[T3], RC[T5]
:11253 :           ID[T0], ID[T1], ID[T2], ID[T3],
:11254 :           SS, SD, Q, FE, LA, LB, LC
:11255
:11256 :RETURNS:       RETURNS @ 10
:11257
:11258 =00
:11259 ADDD.S: :00-----;
:11260 :           RC[T3] D,          ; SAVE SRC0 <L>
:11261 :           D.DAL.SC,        ; SWAP WORD OF SRC0 <L>
:11262 :           SC.K[.FFF9],       ; SETUP SHIFT AMOUNT -7
:11263 :           CALL,J/UNPACK       ; CALL UNPACK DOUBLE FLOATING PT OPERANDS ROUTINE
:11264
:11265 :01-----; RETURN1, SRC = 0, DST MAY BE 0
:11266 :           ALU_D,           ; SET COND CODES AS DST (UNPACK ASSURES CLEAN 0)
:11267 :           SET.CC(INST),     ; SET TR DEP COND CODES
:11268 :           RETURN10          ; GOTO WRITE DEST
:11269
:11270 :10-----; RETURN2, DST = 0, SRC.NE.0
:11271 :           RC[T1] LC,         ; RC1 GETS SRC0 <L>
:11272 :           IR1?, J/ADDD.8    ; ADDD OR SUBD?
:11273
:11274 :11-----; RETURN3, SRC.NE.0, DST.NE.0
:11275 :           ALU_D, RC[T1],     ; LATCH UP PACKED HI DEST IN LC
:11276 :           EALU?, J/ADDD.10   ; BEN ON EALU<N,Z>, SS
:11277 =;END
:11278
:11279 :10-----; CONSTRAINED BLOCK FOR IR1?
:11280 :ADDD.8: :0-----; ADDD: RESULT = SRC, SET COND CODES
:11281 :           ALU_D, SET.CC(INST), ; GOTO WRITE DEST
:11282 :           RETURN10          ;
:11283
:11284 :1-----; SUBD: RESULT = -SRC
:11285 :           D.D.XOR.K[.8000], ; RESULT = -SRC
:11286 :           SET.CC(INST),     ; SET COND CODES
:11287 :           RETURN10          ; GOTO WRITE DEST
:11288 =;END
  
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U 0580, 0D01,003D,BD80,F998,0084,66CA  
 U 0581, 0001,C03E,0180,F800,0070,0010  
 U 0582, 0010,0938,0180,F988,0000,05B2  
 U 0583, 0000,123C,0180,F908,0000,0182  
 U 0582, 0001,C03E,0180,F800,0070,0010  
 U 0583, 0819,C022,4580,F800,0070,0010

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1WT24.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : ADDD, SUBD

D 8

Fiche 2 Frame D8

Sequence 300

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	:11289 :	MAIN BRANCHING POINT OF ADDD - ALSO USED BY POLYD AND ACBD
	:11290 :	AT THIS POINT, MACHINE STATE IS AS FOLLOWS
	:11291 :	D=DST FRAC<L>, Q&ID[T2]=SRC FRAC<L>, RC[T5]&ID[T1]=DST FRAC<H>,
	:11292 :	ID[T0]=SRC FRAC<H>, SC=DST EXP, FE=NABS(SRC EXP - DST EXP),
	:11293 :	SD=DST SGN, SS=DST SGN .XOR, SRC SGN .XOR, SUBD,
	:11294 :	RC[T0]=ORIG SRC<H>, L[&RC[T1]]=ORIG DST<H>, RC[T6]=ORIG DST<L>,
	:11295 :	STATE<0> = POLYD FLAG, STATE<3:1> = 0.
	:11296 :	
	:11297 =000010	
	:11298 ADDD.10:0010-----	DST EXP > SRC EXP, ADD
	:11299 R[R15]_D,	SAVE DST FRAC <L>
U 0182, 0C01,003D,C1F0,2EF8,0081,04AE	:11300 D_Q,	SETUP FOR ALIGN SRC FRAC
	:11301 SC_FE,	GET SHIFT AMOUNT
	:11302 Q_ID[T0],	GET SRC FRAC <H>
	:11303 CALL[ALNPOS]	GO ALIGN SRC
	:11304 :0011-----	DST EXP > SRC EXP, SUB
	:11305 R[R15]_D,	SAVE DST FRAC <L>
	:11306 D_Q,	SETUP FOR ALIGN SRC FRAC
U 0183, 0C01,003D,C1F0,2EF8,0081,080E	:11307 SC_FE,	GET SHIFT AMOUNT
	:11308 Q_ID[T0],	GET SRC FRAC <H>
	:11309 CALL[ALNNEG]	TWO'S COMPLEMENT AND ALIGN SRC
	:11310 ADDD.14:0110-----	DST EXP = SRC EXP, ADD
	:11311 R[R15]_D+Q,	ADD FRAC <L>'S
U 0186, 001D,0014,C5F0,2EF8,0090,C7BD	:11312 Q_ID[TT],	Q GETS DST FRAC <H>
	:11313 C[K].UBCC,	CLOCK IN CARRY IF ANY
	:11314 SC_SC+1,	ADD 1 TO RESULT EXP TO CFF SET SHF.VAL COUNTING
	:11315 J/ADDD.26	
	:11316 ADDD.16:0111-----	DST EXP = SRC EXP, SUB
	:11317 R[R15]_D-Q,	SUB FRAC <L>'S
U 0187, 001D,0000,C5F0,2EF8,0090,C7DA	:11318 Q_ID[TT],	Q GETS DST FRAC <H>
	:11319 C[K].UBCC,	CLOCK IN CARRY IF ANY
	:11320 SC_SC+1,	ADD 1 TO RESULT EXP TO OFFSET SHF.VAL COUNTING
	:11321 J/ADDD.30	
	:11322 :1010-----	DST EXP < SRC EXP, ADD
U 0 1, 0000,003D,C5F0,2D00,0081,04AE	:11323 SC_FE,	SC GETS SHIFT AMOUNT FOR ALIGNMENT
	:11324 Q_ID[T1], LC_RC[T0],	Q GETS DST FRAC <H>, LC GETS SRC EXP
	:11325 CALL[ALNPOS]	GO ALIGN DST
	:11326 :1011-----	DST EXP < SRC EXP, SUB
	:11327 SC_FE,	SC GETS SHIFT AMOUNT FOR ALIGNMENT
	:11328 Q_ID[T1], LC_RC[T0],	Q GETS DST FRAC <H>, LC GETS SRC EXP
U 0188, 0000,003D,C5F3,2D00,0081,080E	:11329 SD NOT.SD,	RESULT SIGN IS SRC SIGN
	:11330 CALL[ALNNEG]	TWO'S COMP AND ALIGN DST
	:11331	
	:11332	
	:11333	
	:11334	
	:11335	

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204]  
: P1W124.MCR 600,1204] MICR02 1L(03) F & D floating point : ADDD, SUBD

F & D floating point 14-Jan-82  
14-Jan-82 15:30:16

E 8

Fiche 2 Frame E8

Sequence 301

VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124

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: FLOAT .MIC [600,1204]

U 0192, 0C00,003C,C9F8,3C00,0181,079E

U 0193, 0C03,0028,C9C0,3C00,0181,079E

U 019A, 0C01,003C,01F8,F990,0181,07B9

U 019B, 0C01,003C,0180,F990,0181,07B1

U 01A3, 0C00,003C,C9E0,3C00,0000,07A9

U 01AB, 0C01,003C,C9F0,2D90,0000,07BA

U 01B3, 0011,1738,01C0,F930,0088,6428

U 01BB, 0C00,003C,C9F0,2C00,0100,C57B

:11336 ; ADDD - RETURNS FROM ALIGNMENT ROUTINE

:11337

:11338 =010010 :----- DST EXP > SRC EXP, ADD, DIFF<32  
:11339 SC FE, FE\_SC, D\_Q, Q\_0. ; SC GETS SHIFT AMT, FE GETS DST EXP,  
:11340 ID[T2]\_D, J/ADDD.21 ; PREPARE TO SHIFT HIGH-ORDER SRC

:11341

:11342 :----- DST EXP > SRC EXP, SUB, DIFF<32  
:11343 SC FE, FE\_SC, D\_Q. ; SC=SHIFT AMT, FE=DST EXP,  
:11344 ALU\_-1, Q\_ALU, ; SIGN-EXTENSION OF FRACT TO Q, PREPARE  
:11345 ID[T2]\_D, J/ADDD.21 ; TO SHIFT HIGH-ORDER NEGATED SRC FRAC

:11346

:11347 =011010 :----- DST EXP < SRC EXP, ADD, DIFF<32  
:11348 SC FE, FE\_SC, D\_Q, Q\_0. ; SC=SHIFT AMT, FE=SRC EXP, PREPARE  
:11349 RC[T2]\_D, J/ADDD.24 ; TO SHIFT HIGH-ORDER DST FRAC

:11350

:11351 :----- DST EXP < SRC EXP, SUB, DIFF<32  
:11352 SC FE, FE\_SC, D\_Q. ; SC=SHIFT AMT, FE=SRC EXP, PREPARE  
:11353 RC[T2]\_D, J/ADDD.23 ; TO SHIFT HIGH-ORDER NEGATED DST FRAC

:11354

:11355 =100011 :----- DST EXP > SRC EXP, ADD/SUB, 32<=DIFF<64  
:11356 ID[T2]\_D, Q\_D, D\_Q. ; SAVE LOW ALIGNED SRC, D GETS SIGN EXT  
:11357 J/ADDD.22

:11358

:11359 =101011 :----- DST EXP < SRC EXP, ADD/SUB, 32<=DIFF<64  
:11360 RC[T2]\_D, Q\_ID[T2], ; SAVE LOW ALIGNED DST, Q GETS LOW SRC.  
:11361 D\_Q, J7ADDD.25 ; D GETS 32\*DST FRAC SIGN

:11362

:11363 =110011 :----- DST EXP > SRC EXP, ADD/SUB, DIFF>63  
:11364 Q\_RC[T6], SC D(EXP)(A), ; D HAS ORIG DST<H>, SET Q TO ORIG DST<L>  
:11365 STATE0?, J/ADDD.20 ; CHECK TO SEE IF WE WERE CALLED FROM POLYD

:11366

:11367 =111011 :----- DST EXP < SRC EXP, ADD/SUB, DIFF>63  
:11368 D\_Q, Q\_ID[T2], FE\_SC+1, ; ANSWER IS +/- SRC - RECONSTRUCT FROM FRAC&EXP  
:11369 J7ADDD.31 ; TO GET SIGN RIGHT (FROM SD) AND BECAUSE  
:11370 ; POLYD DOESN'T HAVE A PACKED VERSION OF SRC.

:11371 =:END

ZZ-ESOAA-124.0 ; FLOAT .1IC [600,1204] F & D floating point 14-Jan-82 F 8  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Sequence 302  
 ; FLOAT .MIC [600,1204] F & D floating point : ADDD, SUBD Page 301

U 0428, 0001,203E,0180,F988,0000,0010 :11372 \*\*\*\*0  
 :11373 ADDD.20:;0-----: HERE WHEN SRC=0 W.R.T. DST AND NOT POLYD  
 :11374 RC[T1]\_Q, RETURN10 ; STORE DST<L> IN RESULT<L> AND EXIT  
 :11375  
 :11376 : \*\*\*\*\*  
 :11377 : \* Patch no. 031, PCS 0428 trapped to WCS 1163 \*  
 :11378 : \*\*\*\*\*  
 :11379  
 U 0429, 0C00,143E,01E0,F800,0000,0010 :11380 :1-----: HERE WHEN SRC=0 W.R.T. DST AND INST IS POLYD  
 :11381 D\_Q, Q\_D, SC?, RETURN10 ; PUT RESULT IN <Q,D> & RETURN (12)  
 :11382 =:END  
 :11383 ADDD.21:-----: HERE WHEN SRC IS TO BE ALIGNED <32 PLACES  
 :11384 D\_DAL.SC, : D GETS ALIGNED SRC FRAC <H>  
 :11385 SC\_FE, : SC GETS BACK DST EXP  
 :11386 Q\_ID[T2] : Q GETS DST FRAC <L>  
 :11387  
 U 07A9, 0D00,003C,C9F0,2C00,0081,07A9 :11388 ADDD.22:-----: HERE WHEN SRC FRACTION IS ALIGNED  
 :11389 ID[T0] D, : ID[T0] GETS ALIGNED SRC FRAC <H>  
 :11390 D\_RC[R15], : D GETS DST FRAC <H>  
 :11391 J7ADDD.14 : GOTO ADD FRAC <L>  
 :11392  
 U 07B1, 0003,0028,01C0,F800,0000,07B9 :11393 ADDD.23:-----: UGLY STATE  
 :11394 ALU\_-1, Q\_ALU : COULDN'T DO THIS AND SAVE DST<L> IN RC[T2]  
 :11395 : IN THE SAME STATE  
 :11396  
 U 07B9, 0D00,003C,C9F0,2C00,0081,07BA :11397 ADDD.24:-----: HERE TO COMPLETE DST ALIGN OF <32 BITS  
 :11398 D\_DAL.SC, : D GETS ALIGNED DST FRAC <H>  
 :11399 SC\_FE, : SC GETS SRC EXP  
 :11400 Q\_ID[T2] : Q GETS SRC FRAC <L>  
 :11401  
 U 07BA, 0810,0038,C580,3D10,0000,0186 :11402 ADDD.25:-----: HERE WHEN DST FRAC IS ALIGNED  
 :11403 ID[T1] D, : STORE ALIGNED DST FRAC <H>  
 :11404 D\_RC[T2], : D GETS ALIGNED DST FRAC <L>  
 :11405 J7ADDD.14 : GOTO ADD FRAC <L>

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 G 8  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 02, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : ADDD, SUBD Fiche 2 Frame G8 Sequence 303  
 Page 302

:11406 ;COME HERE FROM ADDD.14 AFTER ADDING LOW-ORDER FRACTIONS WHEN REAL OPERATION  
 :11407 ; IS SUBTRACT WITH UNEQUAL EXPONENTS OR ADD.  
 :11408  
 :11409 ADDD.26:  
 :11410 D\_Q,  
 :11411 Q\_ID[T0].  
 :11412 FE SC,  
 :11413 C3T?  
 :11414  
 :11415 =0\*  
 :11416 D\_D+Q,  
 :11417 LAB\_R[R15], CLK.UBCC,  
 :11418 J/ADDD.27  
 :11419  
 :11420 :1--  
 :11421 D\_D+Q+1,  
 :11422 LAB\_R[R15], CLK.UBCC  
 :11423 =:END  
 :11424  
 :11425 ADDD.27:  
 :11426 Q\_LA,  
 :11427 A[U?], J/ADDD.31  
 :11428  
 :11429 ;COME HERE FROM ADDD.16 AFTER SUBTRACTING LOW-ORDER FRACTIONS  
 :11430 ;WHEN REAL OPERATION IS SUBTRACT WITH EQUAL EXPONENTS.  
 :11431  
 :11432 ADDD.30:  
 :11433 D\_Q,  
 :11434 Q\_ID[T0].  
 :11435 C31?  
 :11436  
 :11437 =0\* :0--  
 :11438 D\_D-Q-1,  
 :11439 CLK.UBCC  
 :11440 LAB\_R[R15].  
 :11441 J/ADDD.32  
 :11442  
 :11443 :1--  
 :11444 D\_D-Q,  
 :11445 CLK.UBCC  
 :11446 LAB\_R[R15]  
 :11447 =:END  
 :11448  
 :11449 ADDD.32:  
 :11450 FE SC,  
 :11451 Q\_R[R15],  
 :11452 A[U?]  
 :11453  
 :11454 =1010 :00--  
 :11455 SD.NOT.SD,  
 :11456 O\_O-Q,  
 :11457 CLK.UBCC  
 :11458 J/ADDD.33  
 U 07BD, 0C00,033C,C1F0,2C00,0100,0420  
 U 0420, 081D,0014,0180,FA78,0010,07CA  
 U 0422, 081D,0010,0180,FA78,0010,07CA  
 U 07CA, 0000,1B3C,01C0,F800,0000,067B  
 U 07DA, 0C00,033C,C1F0,2C00,0000,0474  
 U 0474, 081D,0008,0180,FA78,0010,07DC  
 U 0476, 081D,0000,0180,FA78,0010,07DC  
 U 07DC, 0000,1B3C,01C0,FA78,0100,067A  
 U 067A, 001F,0000,01C3,F800,0010,07E5

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
; FLOAT .MIC [600,1204] F & D floating point : ADDD, SUBD

H 8

Fiche 2 Frame H8

Sequence 304

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:11459 ; ALL ADDS AND SUBTRACTS CONVERGE IN ONE OF THE NEXT TWO STATES.  
:11460 ; EMODD ALSO ENTERS HERE TO NORMALIZE AND PACK ITS FRACTION RESULT.  
:11461  
:11462 =1011  
:11463 ADDD.31:01-----: RESULT FRAC <H> IS NOT 0  
:11464 SC SHF.VAL. : POS DIFF, NORMALIZE RESULT  
:11465 D BAL.NORM. : D GETS NORMALIZED FRAC <H>  
U 067B, 0E00,003C,0180,F800,008C,67E8  
:11466 J7ADDD.36  
:11467  
:11468 =1111 :11-----: RESULT FRAC <H> IS 0  
:11469 SC-SC-K[.20],  
:11470 FE-SC-K[.20],  
:11471 D 0.0.0,  
:11472 J7ADDD.31  
:11473 =:END : ADJUST EXP  
: COUNT THE DUMMY LEADING 0  
: SET FRAC <H>, CLR FRAC <L>

U 067F, 0C00,003C,75F8,F800,0184,A67B

I 8

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Sequence 305  
 ; FLOAT .MIC [600,1204] F & D floating point : ADDD, SUBD Page 304

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:11474 ADDD.33:-----
:11475   D NOT.D,CLK.UBCC,    ; 1'S COMP OF FRAC <H>
:11476   Z?                   ; IS LOW FRAC ALL ZEROS?
:11477
:11478 =0      :0-----;
:11479   ALU?,J/ADDD.31      ; IS DIFF ZERO?
:11480
:11481   ;1-----;
:11482   D D+K[.1],          ; YES, FRAC <L> = 0, MAKE 2'S COMP OF FRAC <H>
:11483   J7ADDD.31
:11484 =:END
:11485
:11486 ADDD.36:-----
:11487   R[R15] D,           ; COME HERE WITH FRAC<H> NORMALIZED
:11488   D_Q.Q_0              ; SAVE FRAC <H>
:11489
:11490   ;-----;
:11491   D_DAL.SC,           ; SETUP FOR NORMALIZE FRAC <L>
:11492   SC_FE,FE_SC,         ; SC GETS EXP, FE GETS #OF LEADING ZEROS
:11493   Q_R[R15]             ; Q GETS BACK FRAC <H>
:11494
:11495   ;-----;
:11496   SC_SC-FE,           ; EXP_EXP - #OF LEADING ZEROS
:11497   D_Q.Q_0
:11498   R[R15] D
:11499
:11500   ;-----;
:11501   LAB_R[R15]
:11502   ALU_LA[OR]D,CLK.UBCC, ; LATCH FRAC <L>
:11503   FE_R[.18]             ; CHECK IF RESULT FRAC'S ARE ZEROS
:11504
:11505   ;-----;
:11506   K[.80].               ; SET FE TO 24. FOR PACKING DOUBLE RESULT
:11507   Z?
:11508 =0      :0-----;
:11509   Q_LA+K[.80],          ; PRESET SLOW CONSTANT FOR ROUNDING
:11510   C[K].UBCC,            ; RESULT FRAC'S = 0
:11511   J/PACKD               ; ADD 80(HEX) FOR ROUNDING
:11512
:11513   ;-----;
:11514   SC_K[ZERO]            ; CLOCK IN FOR CARRY IF ANY
:11515   RC[T1] K[ZERO],D_0,    ; GOTO PACK DOUBLE FLOATING RESULT
:11516   SET.CC(INST),          ; RESULT FRAC'S = 0
:11517   STATE0?                ; RESULT SET TO 0
:11518
:11519   ;-----;
:11520 =****0      :0-----;
:11521   RETURN10               ; SET COND CODES
:11522
:11523
:11524   ;-----;
:11525   RETURN12               ; SEE IF WE WERE CALLED FROM POLYD
:11526 =:END
  
```

U 07E5, 0801,0128,0180,F800,0010,042C  
 U 042C, 0000,1B3C,0180,F800,0000,0678  
 U 042D, 0819,0014,0580,F800,0000,0678  
 U 07E8, 0C01,003C,01F8,FAF8,0000,07F5  
 U 07F5, 0D00,003C,01C0,FA78,0181,07FE  
 U 07FE, 0C01,003C,01F8,FAF8,0080,A806  
 U 0806, 001C,2030,7D80,FA78,0114,680A  
 U 080A, 0000,013C,4180,F800,0000,0440  
 U 0440, 0018,0014,41C0,F800,0010,03FC  
 U 0441, 0F18,D738,1980,F988,00F4,644C  
 U 044C, 0000,003E,0180,F800,0000,0010  
 U 044D, 0000,003E,0180,F800,0000,0012

11527 : ADDD/SUBD ALIGNMENT SUBROUTINE  
 11528 : ENTER FROM ADDD.10 BRANCH TARGETS WITH <Q,D> = FRACTION TO BE ALIGNED,  
 11529 : FE = SC = AMOUNT TO ALIGN IT, LC(EXP) = LARGER OF (SRC EXP, DST EXP)  
 11530 : ENTRY IS AT ALNNEG IF <Q,D> SHOULD BE NEGATED FIRST, ELSE AT ALNPOS.  
 11531 : THERE ARE SEVERAL RETURN POINTS:  
 11532 : RETURN10 EXP DIFF < 32 - D HAS ALIGNED FRAC<L>, SC HAS LC(EXP)  
 11533 : RETURN21 32<=EXP DIFF<64 - <Q,D> HAS ALIGNED FRAC, SC HAS LC(EXP)  
 11534 : RETURN31 EXP DIFF > 63 - <Q,D>=<BIG OP<H>, SRC FRAC<H>, SC=LC(EXP)  
 11535 : NOTE: MAX EXP DIFF IS 53 (INSTEAD OF THE USUAL 57) BECAUSE POLYD USES ADDD  
 11536 :  
 11537 :  
 U 080E, 081F, 2000, 0180, F800, 0010, 0816  
 11538 :  
 11539 : ALNNEG: D\_O-D, CLK.UBCC ; NEGATE FRACTION - LOW ORDER FIRST  
 11540 :  
 U 0816, 001F, 0300, 01C0, F800, 0000, 04AC  
 11541 :  
 11542 : Q\_O-Q, C31? ; NEGATE HI-ORDER AND CHECK FOR BORROW  
 11543 :  
 U 04AC, 0019, 2000, 05C0, F800, 0000, 04AE  
 11544 : =0\* :0-----; BORROW  
 11545 : Q\_Q-K[.1] ; OK, BORROW!  
 11546 :  
 U 04AE, 0000, 003C, 8D80, F800, 0094, 881E  
 11547 :  
 11548 : ALNPOS: SC\_SC+K[.1F], CLK.UBCC ; SET EALU.N IF EXP DIFF => 32  
 11549 :  
 11550 :  
 U 081E, 0000, 123C, 7580, F800, 0095, 8546  
 11551 : EALU\_SC+K[.20], CLK.UBCC, ; SET EALU.N IF EXP DIFF > 63  
 11552 : SC\_FE, EALU? ; RESTORE ORIG EXP DIFF, TEST DIFF=>32  
 11553 :  
 11554 : =0110 :00-----; EXP DIFF < 32, FRACTION POSITIVE  
 11555 : D\_DAL.SC, SC\_LC(EXP), ; D GETS LOW-ORDER ALIGNED FRAC  
 11556 : RETURN[10] ;  
 11557 :  
 11558 :  
 U 0546, 0D10, 003A, 0180, F800, 0083, 0010  
 11559 : :01-----; EXP DIFF < 32, FRACTION NEGATIVE  
 11560 : D\_DAL.SC, SC\_LC(EXP), ; NEGATIVE SC MEANS - LET THE CALLER WORRY  
 11561 : RETURN[10] ;  
 11562 :  
 U 0547, 0D10, 003A, 0180, F800, 0083, 0010  
 11563 : :10-----; EXP DIFF => 32, FRACTION POSITIVE  
 11564 : SC\_SC+K[.20], D\_Q, Q\_O, ; SHIFT FRACT 32 PLACES RIGHT, REDUCE AMT BY 32  
 11565 : EALU.N?, J/ALN.01 ; TEST IF EXP DIFF > 63  
 11566 :  
 U 054E, 0C00, 123C, 75F8, F800, 0084, 8557  
 11567 : :11-----; EXP DIFF => 32, FRACTION NEGATIVE  
 11568 : SC\_SC+K[.20], D\_Q, ; SHIFT FRACT 32 BITS RT, REDUCE SHFTCT BY 32  
 11569 : ALU\_-1, Q\_ALU, EALU.N? ; SIGN-EXTEND FRACT, TEST IF EXP DIFF > 63  
 11570 : =:END ;  
 11571 :  
 U 0557, 0D10, 003A, 0180, F800, 0083, 0021  
 11572 : =0111 :0-----; 32<= EXP DIFF <= 63  
 11573 : ALN.01: D\_DAL.SC, SC\_LC(EXP), ; <Q,D> HAVE ALIGNED SIGN-EXTENDED FRACT  
 11574 : RETURN[21] ; SC HAS BIGGER EXP - RETURN  
 11575 :  
 U 055F, 0810, 003A, C1F0, 2C00, 0083, 0031  
 11576 : :1-----; 63 < EXP DIFF  
 11577 : D\_LC, SC\_LC(EXP), ; HOPELESS - D GETS BIGGER OPERAND<H>  
 11578 : Q\_ID[0], RETURN[31] ; SC GETS BIGGER EXP, Q GETS SRC FRAC<H>

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 K 8  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : MULD

Fiche 2 Frame K8 Sequence 307  
 Page 306

U 0228, 0000,003C,19E0,F988,1404,6325

```
:11579 .TOC   "      F & D floating point : MULD"
:11580
:11581 ;MULD, *-R
:11582 ;ENTER HERE AT B.FORK WITH SRC0 IN <RC0, D>, R IN LA, LB.
:11583 ;LEAVE HERE WITH SRC0 IN <RC0, Q>, DST0 IN <RC1, D> TO GOTO SAME FLOW
:11584 ;AS ***, ***-**.
:11585
:11586 228: -----
:11587     STATE K[ZERO],          : CLR POLYD FLAG
:11588     RC[T1]_LA,             : RC1 GETS DST0 <H>
:11589     Q_D                  : Q GETS DST0 <L>
:11590
:11591 =0**** :0-----
:11592     D_R(PRN+1)            : D GETS DST0 <L>
:11593     STATE K[ZERO],          : CLR FLAG FOR POLYD
:11594     CALL,J/MULD.00        : CALL MULD SUBROUTINE
:11595
:11596     ;1-----: RETURN WITH RESULT IN <D, RC1>
:11597     R(PRN)_D,              : STORE RESULT <H>
:11598     J/ADDD_P               : GOTO STORE RESULT <L>
:11599 =:END
:11600
:11601
:11602 ;DOUBLE FLOATING POINT ARITHMETIC MULD.
:11603 ;ENTER FROM DP WITH SRC OPD IN <RC0, Q>, DST OPD IN <RC1, D>.
:11604 ;ALWAYS YIELDS NORMALIZED AND ROUNDED RESULT.
:11605
:11606 38C:
:11607 MULD: :0-----
:11608     STATE K[ZERO],          : CLR FLAG FOR POLYD
:11609     CALL,J/MULD.00        : CALL MULD SUBROUTINE
:11610
:11611 39C: :1-----: WRITE RESULT
:11612
```

U 0325, 0800,003D,1980,F860,1404,7003

U 0335, 0001,003C,0180,F8D8,0000,0796

U 038C, 0000,003D,1980,F800,1404,7003

U 039C, F000,003F,01F0,F847,0000,0300

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : DIVD

L 8

Fiche 2 Frame L8

Sequence 308

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U 0229, 0000,003C,01E0,F988,0000,082A

U 082A, 0800,003C,0180,F860,0000,0360

U 0360, 0C01,003D,6580,F980,0084,6608

U 0370, 0001,5A3C,0180,F800,0050,00FC

U 038B, 0C01,003D,6580,F980,0084,6608

U 039B, 0001,5A3C,0180,F800,0050,005C

U 005C, F000,003F,01F0,F847,0000,0300

U 005E, F000,003F,01F0,F847,0020,0300

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:11613 .TOC   "      F & D floating point : DIVD"
:11614
:11615 :DIVD, *-R
:11616 :ENTER HERE AT B.FORK WITH SRC0 IN <RC0, D>, R IN LA, LB.
:11617 :LEAVE HERE WITH SRC0 IN <RC0, Q>, DST0 IN <RC1, D> TO GOTO SAME FLOW
:11618 :AS ***, ***-**.
:11619
:11620 229: -----
:11621     RC[T1]_LA,          : RC1 GETS DST0 <H>
:11622     Q_D                 : Q GETS DST0 <L>
:11623
:11624 -----: D_R(PRN+1)       : D G/T S DST0 <L>
:11625
:11626 =0****:0-----:
:11627     RC[T6]_D,          : SAVE DST0 <L>
:11628     D_Q,                : D GETS SRC0 <L>
:11629     SC_K[.10],          : SC GETS 16. FOR SWAP WORD OF FRAC <L>
:11630     CAEL,J/DIVD.S      : CALL DIVD SUBROUTINE
:11631
:11632     ;1-----: RETURN WITH RESULT IN <D, RC1>
:11633     ALU.D,N&Z ALU.V&C_0, : SET COND CODES N,Z
:11634     WORD,PSL.V?,J/ADDD.M : GOTO STORE RESULT <H,L>
:11635
:11636 =:END
:11637
:11638
:11639 :DOUBLE FLOATING POINT DIVD.
:11640 :ENTER FROM DP WITH SRC OPD IN <RC0, Q>, DST OPD IN <RC1, D>.
:11641 :QUOT = DST/SRC = <RC1, D>
:11642 :ALWAYS YIELDS NORMALIZED AND ROUNDED RESULT.
:11643
:11644
:11645 38B: -----
:11646     DIVD: -----
:11647     RC[T6]_D,          : SAVE DST0 <L>
:11648     D_Q,                : D GETS SRC0 <L>
:11649     SC_K[.10],          : SC GETS 16. FOR SWAP WORD OF FRAC <L>
:11650     CAEL, J/DIVD.S      : CALL DIVD SUBROUTINE
:11651
:11652 39B: -----
:11653     ALU.D,N&Z ALU.V&C_0, : SET COND CODES N,Z
:11654     WORD,PSL.V?          : HAS TO RESET PSL<V>?
:11655
:11656 =110*:0-----: NO:
:11657     WRITE.DEST,J/WRD    : WRITE RESULT
:11658
:11659     ;1-----: YES:
:11660     SET.V,               : RESET PSL <V>
:11661     WRITE.DEST,J/WRD    : WRITE RESULT
:11662 =:END

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ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 Fiche 2 Frame M8 Sequence 309  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 308  
 : FLOAT .MIC [600,1204] F & D floating point : DIVD

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:11663 :DOUBLE FLOATING POINT DIVD ROUTINE.
:11664
:11665 :ALGORITHM: NON-RESTORING DIVIDE IN TWO LOOPS, ONE FOR THE FIRST 32 BITS
:11666 : OF QUOTIENT AND ONE FOR THE NEXT 26 BITS.
:11667
:11668 :INPUTS: RC[T0] = SRC<H>
:11669 : D = Q = SRC<L>
:11670 : RC[T1] = DST<H>
:11671 : RC[T6] = DST<H>
:11672 : SC = 10 (HEX)
:11673
:11674 :OUTPUTS: D = PACKED ROUNDED QUOTIENT<H>
:11675 : RC[T1] = PACKED ROUNDED QUOTIENT<L>
:11676 : CONDITION CODES AND ID[CES] SET UP FROM QUOTIENT
:11677
:11678 :TEMPORARIES: R[R15], RC[T2], RC[T3], RC[T4], RC[T5],
:11679 : ID[T0], ID[T1], ID[T2], ID[T3], ID[T4],
:11680 : SS, SD, Q, FE, LA, LB, LC
:11681 : (R[R1] IS USED INTERNALLY, BUT IT IS SAVED FIRST & RESTORED AFTER)
:11682
:11683 :RETURNS: RETURNS @ 10
:11684
:11685 =00
:11686 DIVD.S: :00-----
:11687 :RC[T3] D, : SAVE SRC0 <L>
:11688 :D DAL.SC : SWAP WORD OF SRC0 <L>
:11689 :SC K[.FFF9], : SETUP SHIFT AMOUNT -7
:11690 :CALL,J/UNPACK : CALL UNPACK DOUBLE FLOATING PT OPERANDS ROUTINE
:11691
:11692 :01-----: RETURN1, SRC = 0, DST MAY BE 0
:11693 :D K[.8000], : DIVISOR IS 0, NO DIV
:11694 :NZ ALU.VBC_0,WORD, : COND CODES SET BY D'END
:11695 :J/DIVD.20
:11696
:11697 :10-----: RETURN2, SRC.NE.0, DST = 0
:11698 :RC[T1] K[ZERO], D_0, : RESULT QUOTIENT IS 0
:11699 :NZ ALU.VBC_0, : COND CODES SET BY D'END
:11700 :RETURN10 : GOTO WRITE RESULT
:11701
:11702 :11-----: RETURN3, SRC.NE.0, DST.NE.0
:11703 :ID[T4] D, : SAVE DST (D'END) FRAC <L>
:11704 :D R[R1], : D GETS R1
:11705 :SD_SS, SC_FE : SD, SC GET RESULT SIGN, EXP
:11706 =:END
:11707
:11708 :-----: FIX RESULT SIGN
:11709 :SD NOT SD, : SAVE R1
:11710 :ID[T3] D, : GET SRC (D'SOR) FRAC <L>
:11711 :R[R15]_Q
:11712
:11713 :-----: Q GETS DST (D'END) FRAC <L>
:11714 :Q_ID[T4] : LB GETS SRC (D'SOR) FRAC <L>
:11715 :LAB R[R15]. : CLR POLYD FLAG
:11716 :STATE_0(A)
  
```

U 0608. 0D01.003D,BD80,F998,0084,66CA  
 U 0609. 0818.4038,4580,F800,0050,0470  
 U 06CA. 0F18.003A,1980,F988,0050,0010  
 U 0608. 0800.003C,D184,3E08,0081,082E  
 U 082E. 0001.203C,CD83,3EF8,0000,0832  
 U 0832. 0003.003C,D1F0,2E78,1408,6836

U 0836, 0001.203C,C1F0,2E88,0000,083A	:11717	-----;	
	:11718	Q_ID[T0],	; Q GETS D'SOR FRAC <H>
	:11719	R[R1]_Q	; R1 GETS D'END FRAC <L>
	:11720	-----;	
	:11721	-----;	
	:11722	R[C[T4]_Q,	; RC4 GETS D'SOR <H>
	:11723	Q_ID[TT]	; Q GETS DST (D'END) FRAC <H>
	:11724	-----;	
	:11725	-----;	
	:11726	[LA_RA[R1]]	; LATCH D'END FRAC <L>
	:11727	-----;	
	:11728	-----;	
	:11729	SC_SC+K[.80],	ADD EXP BIAS 128. TO RESULT EXP
	:11730	D_Q_0_0	D GETS D'END FRAC <H>. CLR QUOT BITS
	:11731	LC_RC[T4]&R1_(LA-LB).LEFT	; LC GETS D'SOR<H>, R1 GETS IMMED D'END FRAC<L>
	:11732	SI7ZERO,	SHIFT IN ZEROS
	:11733	SET.CC(LONG)	; SET PSL<N,C> BITS
	:11734	-----;	
	:11735	-----;	
	:11736	ALU_D[INST.DEP]LC,	SUBT HIGH FRACS
	:11737	D_ALU.LEFT.SI/DIVL.	
	:11738	Q_Q.LEFT,	SHIFT IN QUOT BIT
	:11739	LA_RA[R1].	LATCH D'END FRAC <L>
	:11740	CLR.UBCC	FLAG FOR NEXT OPERATION, + OR -
U 084E, 0C2C.0000,41F8,FBA0,00F4,8852	:11741	FE_K[.1E]	SET LOOP CT FOR 31 LOOPS
	:11742	-----;	
	:11743	-----;	
	:11744	SI_FE,RC[T2]_K[SC].	SC GETS 30., SAVE RESULT EXP IN RC2
	:11745	C3T?	+ OR - ?
	:11746	=0*	
	:11747	-----;	
	:11748	LC_RC[T4]&R1_(LA-LB).LEFT	; R1 GETS IMMEDIATE D'END FRAC <L>
	:11749	SI7ZERO,	SHIFT IN ZEROS
	:11750	SET.CC(LONG),	SET PSL<N,C> BITS
	:11751	SC_SC+1	INC COUNTER BY 1 SINCE 1ST QUOT BIT IS 0
	:11752	J/DIVD.08	GOTO ADD HIGH FRACS
	:11753	-----;	
	:11754	-----;	
	:11755	STATE_K[.80],	SET FLAG TO INC EXP BY 1
	:11756	LC_RC[T4]&R1_(LA-LB).LEFT	; R1 GETS IMMEDIATE D'END FRAC <L>
	:11757	SI7ZERO,	SHIFT IN ZEROS
	:11758	SET.CC(LONG),	SET PSL<N,C> BITS
	:11759	J/DIVD.06	GOTO SUBT HIGH FRACS
	:11760	=:END	
	:11761	=*0*	
	:11762	DIVD.04:0-----;	FIRST 32 QUOT BITS DONE
	:11763	SC_K[.1A],	SHIFT AMOUNT FOR LOWER QUOTIENT BITS
	:11764	R[R15]_Q,	SAVE HIGH QUOT FRAC BITS
	:11765	Q_0	CLR QUOT FOR ADDITIONAL QUOT BITS
	:11766	C31?, J/DIVD.10	+ OR - FOR NXT QUOT BIT?
	:11767	-----;	
	:11768	-----;	
	:11769	FE_K[.8].	PRE-SET SHIFT AMOUNT
	:11770	C3T?	NXT OPERATION, + OR - ?
	:11771	=:END	

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204]  
; P1WT24.MCR 600,1204] MICRO2 1L(03) F & D floating point : DIVD

F & D floating point 14-Jan-82  
14-Jan-82 15:30:16

B 9  
Fiche 2 Frame B9  
VAX11/780 Microcode : PCS 01, FPLA OE, WCST24

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U 04CC, 002C.0014.0580,FBA0,00F4,A89A

:11772 =0\* :0-----  
:11773 LC RC[T4]&R1\_(LA+LB).LEFT.; R1 GETS IMMEDIATE D'END FRAC <L>  
:11774 SI7ZERO, : SHIFT IN ZEROS  
:11775 SET.CC(LONG), : SET PSL<N,C> BITS  
:11776 SC\_SC-K[.1], : DECREMENT COUNTER BY 1  
:11777 J/DIVD.08 ; GOTO ADD HIGH FRACS

U 04CE, 002C.0000.0580,FBA0,00F4,A865

:11779 :1-----  
:11780 LC RC[T4]&R1\_(LA-LB).LEFT.; R1 GETS IMMEDIATE D'END FRAC <L>  
:11781 SI7ZERO, : SHIFT IN ZEROS  
:11782 SET.CC(LONG), : SET PSL<N,C> BITS  
:11783 SC\_SC-K[.1] : DECREMENT LOOP COUNT

U 0865, 0831,140C,0028,F888,0010,04BC

:11784 =;END  
:11785 DIVD.06:-----  
:11786 ALU\_D[INST.DEP]LC, : SUBT HIGH FRACS  
:11787 D\_A[U.LEFT,SI/DIVD, :  
:11788 Q\_Q.LEFT, : SHIFT IN QUOT BIT  
:11789 LA\_RA[R1], : LATCH D'END FRAC <L>  
:11790 CLR.UBCC, : FLAG FOR NEXT OPERATION, + OR -  
:11791 SC.GT.0?, J/DIVD.04 : END OF 1ST LOOP?

U 089A, 0831,142C,0028,F888,0010,04BC

:11792 :1-----  
:11793 DIVD.08:-----  
:11794 ALU\_D+LC+PSL.C, : ADD HIGH FRACS  
:11795 D\_A[U.LEFT,SI/DIVD, :  
:11796 Q\_Q.LEFT, : SHIFT IN QUOT BIT  
:11797 LA\_RA[R1], : LATCH D'END FRAC <L>  
:11798 CLR.UBCC, : FLAG FOR NEXT OPERATION, + OR -  
:11799 SC.GT.0?, J/DIVD.04 : END OF 1ST LOOP?

U 04DC, 002C.0014.0580,FBA0,00F4,A8A2

:11800 :0\*  
:11801 DIVD.10:-----  
:11802 LC RC[T4]&R1\_(LA+LB).LEFT.; R1 GETS IMMEDIATE D'END FRAC <L>  
:11803 SI7ZERO, : SHIFT IN ZEROS  
:11804 SET.CC(LONG), : SET PSL<N,C> BITS  
:11805 SC\_SC-K[.1], : DECREMENT COUNTER BY 1  
:11806 J/DIVD.12 ; GOTO ADD LOW FRACS

U 04DE, 002C.0000.0580,FBA0,00F4,A89E

:11807 :1-----  
:11808 LC RC[T4]&R1\_(LA-LB).LEFT.; R1 GETS IMMEDIATE D'END FRAC <L>  
:11809 SI7ZERO, : SHIFT IN ZEROS  
:11810 SET.CC(LONG), : SET PSL<N,C> BITS  
:11811 SC\_SC-K[.1] : DECREMENT COUNTER BY 1

U 089E, 0831,140C,0028,F888,0010,04FO

:11812 =;END  
:11813 :-----  
:11814 ALU\_D[INST.DEP]LC, : SUBT HIGH FRACS  
:11815 D\_A[U.LEFT,SI/DIVD, :  
:11816 Q\_Q.LEFT, : SHIFT IN QUOT BIT  
:11817 LA\_RA[R1], : LATCH D'END FRAC <L>  
:11818 CLR.UBCC, : FLAG FOR NEXT OPERATION, + OR -  
:11819 SC.GT.0?, J/DIVD.14 : END OF 2ND LOOP (LOW QUOT BITS) ?

Z7-ESOAA-124.0 ; FLOAT .MIC [600,1204]  
; P1W124.MCR 600,1204]  
; FLOAT .MIC [600,1204]

F & D floating point  
MICR02 1L(03) 14-Jan-82 15:30:16

C 9

14-Jan-82 15:30:16

VAX11/780 Microcode : PCS 01, PLA OE, WCS124

Sequence 312

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F & D floating point : DIVD

U 08A2, 0831,142C,0028,F888,0010,04F0

U 04F0, 0C00,003C,CDF0,2E78,0000,08A6

U 04F2, 0000,033C,0180,F800,0000,04DC

U 08A6, 0001,203C,D5F8,FA88,0084,68AA

U 08AA, 0D10,0038,7D80,F910,0186,68BA

U 08BA, 0800,163C,41E0,F800,0000,02D4

U 02D4, 0019,2014,41C0,F800,0010,03FC

U 02DC, 0019,2014,41C0,F800,0090,C3FC

U 0470, 0818,0039,4580,F800,0000,0E00

U 0471, 0000,003E,0180,F800,0000,0010

:11823 DIVD.12:  
:11824 ALU D+LC+PSL.C,  
:11825 D[A[U.LEFT],SI/DIVD,  
:11826 Q~Q.LEFT,  
:11827 LA R[R1].  
:11828 CLR.UBCC.  
:11829 SC.GT.0?  
:11830 =\*0\* DIVD.14:  
:11831 D.Q,Q\_ID[T3],  
:11832 LAB.R[R15].  
:11833 J/DIVD.16  
:11834  
:11835  
:11836 :1-----  
:11837 C31?, J/DIVD.10  
:11838 =:END  
:11839  
:11840 DIVD.16:  
:11841 R[R1]\_Q,  
:11842 SC\_K[.6],Q\_0  
:11843  
:11844  
:11845 D.DAL.SC,  
:11846 SC\_RC[T2].  
:11847 FE\_K[.18]  
:11848  
:11849 :1-----  
:11850 Q.D.D\_LA.K[.80],  
:11851 STATE7-4?  
:11852  
:11853 =0\*\*\*  
:11854 :0-----  
:11855 Q\_Q+K[.80],CLK.UBCC.  
:11856 J7PACKD  
:11857  
:11858 :1-----  
:11859 SC\_SC+1,  
:11860 Q\_Q+K[.80],CLK.UBCC.  
:11861 J7PACKD  
:11862  
:11863 =:END  
:11864 =0  
:11865 DIVD.20:  
:11866 D\_K[.8000],  
:11867 CALL,J/DIVBY0  
:11868  
:11869 RETURN10  
:11870  
:11871 : \*\*\*\*\*  
:11872 \* Patch no. 071, PCS 0471 trapped to WCS 1190 \*  
:11873 : \*\*\*\*\*  
:11874 =:END

ADD HIGH FRACS  
SHIFT IN QUOT BIT  
LATCH D'END FRAC <L>  
FLAG FOR NEXT OPERATION, + OR -  
END OF 2ND LOOP (LOW QUOT BITS)?  
YES: END OF LOOPS  
D GETS LOW QUOT BITS, Q GETS BACK OLD R1  
LATCH HIGH QUOT BITS  
GOTO PACKING  
NO: NOT END YET  
GOTO +/- FOR NXT QUOT BIT  
RESTORE R1  
SET TO ALIGN LOW QUOT BITS  
SHIFT LOW QUOT BITS TO LEFT  
SC GETS RESULT EXP  
FE GETS 24. FOR NXT SHIFT  
D GETS BACK HIGH QUOT BITS  
INC EXP BY 1?  
Q GETS LOW QUOT FRAC BITS  
GOTO PACKING  
EXP ADJUSTED BY 1  
Q GETS LOW QUOT FRAC BITS  
GOTO PACKING  
FP -0  
GOT TO SET CES FL DIV BY 0

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : UNPACK ONE DOUBLE OPERAND

D 9

Fiche 2 Frame D9

Sequence 313

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:11875 .TOC " F & D floating point : UNPACK ONE DOUBLE OPERAND"  
 :11876 :  
 :11877 :INPUTS: Q = OPERAND<H>  
 :11878 : D = OPERAND<L>  
 :11879 :  
 :11880 :OUTPUTS: SC = EXPONENT  
 :11881 : SS = SD = SIGN  
 :11882 : ID[T1] = RC[T5] = HIGH FRACTION WITH NORMALIZE BIT  
 :11883 : D = LOW FRACTION  
 :11884 :  
 :11885 :TEMPORARIES: R[R15], LA, LB  
 :11886 :  
 :11887 :RETURNS: RETURNS @ 1 IF OPERAND = 0  
 :11888 : RETURNS @ 2 IF OPERAND NON-ZERO  
 :11889 :  
 :11890 :UNPK: :-----:  
 :11891 : R[R15].Q, : R15 GETS OPR<H>  
 :11892 : Q\_D,SC\_K[.10] : READY TO SWAP OPR <L> WORD  
 :11893 :  
 :11894 :UNPK.1: :-----:  
 :11895 : D\_DAL.SC, : LOW FRAC WORD-SWAPPED  
 :11896 : SC\_K[.19], : FOR FRAC <H> ALIGN  
 :11897 : Q\_R[R15](FRAC), : OPR FRAC <H>  
 :11898 : SS\_SS\_XOR\_ALU15&SD\_ALU15, : SET SS/SD  
 :11899 : CHR.FLT.OPR : CHECK FOR OPR = -0  
 :11900 :  
 :11901 :-----:  
 :11902 : D\_DAL.SC, : RIGHT JUSTIFIED FRAC <H>  
 :11903 : Q\_D,SC\_K[.7] : SET FOR LEFT JUSTIFIED FRAC <H>  
 :11904 :  
 :11905 :-----:  
 :11906 : D\_DAL.SC, : D GETS UNPACKED FRAC <H>  
 :11907 : EALU\_R[R15](EXP), : CLOCK IN IF 0 EXP  
 :11908 : CLK.UBCC :  
 :11909 :  
 :11910 :-----:  
 :11911 : ID[T1] D,RC[T5]\_D, : STORE UNPACKED FRAC <H>  
 :11912 : D\_Q,Q\_0, : READY FOR FRAC <L>  
 :11913 : EALU.Z? : EXP 0?  
 :11914 :  
 :11915 :=\*011 :-----:  
 :11916 : D\_DAL.SC, : NO: EXP .NE. 0  
 :11917 : SC\_R[R15](EXP), : D GETS UNPACKED FRAC <L>  
 :11918 : RETURN2 : SC GETS EXP  
 :11919 :  
 :11920 :-----:  
 :11921 : RC[T5]\_K[ZERO],D\_0, : YES: EXP = 0  
 :11922 : SC\_K[ZERO], : RESULT 0  
 :11923 : RETURN1 :  
 :11924 :=:END :

U 08BE, 0001,203C,65E0,FAF8,0084,68DA  
 U 08DA, 0D00,003C,B9CD,FA78,0884,68DE  
 U 08DE, 0D00,003C,5DE0,F800,0084,68FD  
 U 08FD, 0D00,003C,0180,FA78,0018,6911  
 U 0911, 0C01,123C,C5F8,3DA8,0000,03E3  
 U 03E3, 0D00,003E,0180,FA78,0083,0002  
 U 03E7, 0F18,003A,1980,F9A8,0084,6001

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 Fiche 2 Frame E9 Sequence 314  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 313  
 : FLOAT .MIC [600,1204] F & D floating point : CVTBF, CVTWF, CVTLF

E 9

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:11925 .TOC   "      F & D floating point : CVTBF, CVTWF, CVTLF"
:11926
:11927 :11928 CVTB/W/LF (4C/4D/4E) SRC.RX, DST.WF
:ENTER HERE AT B.FORK, WITH D CONTAINS SRC
:11929
:11930 24F: -----
:11931 CVTBF: D.D.SXT[INST.DEP],Q_0, : SIGN EXT SRC TO D
:11932 SET.CC(INST), : SET COND CODES
:11933 CLR.SD&SS, : ASSUME POSITIVE RESULTS
:11934 SC K[E,A0], : SC SET TO BIAS 128 + SHF 32.
:11935 IRT? : IS IT CVTLF?
:11936
:11937 =10 :0-----: NO: IT IS CVTBF/CVTWF
:11938 CVTBF.0:FE SC-SHF.VAL, : ADJUST EXP FOR NORMALIZATION
:11939 D BAL.NORM, : D GETS NORMALIZED FRAC
:11940 SIGNS?,J/CVTBF.1 : BEN ON D.NE.0, D[31]
:11941
:11942 :1-----: YES: CVTLF
:11943 SIGNS?,J/CVTLF.2 : TEST SRC SIGN AND ZERONESS
:11944 =:END
:11945
:11946 =00 :00-----: CONSTRAINT FOR SIGNS; ALSO C31 (SEE CVTBF.5+2)
:11947 CVTBF.1:D_Q, WRITE.DEST : SRC=0 (OR NO OVFLO ON ROUND - SEE CVTBF.5+2)
:11948
:11949 =10 :10-----: SRC IS POS: D GETS PACKED FP RESULT
:11950 EALU FE,D.PACK.FP. : GOTO WRITE RESULT
:11951 W.ITE.DEST
:11952
:11953 :11-----:
:11954 D_0-D.
:11955 SD NOT.SD,
:11956 J/CVTBF.0 : NEGATIVE SOURCE. MAKE IT POSITIVE
:11957 =:END : SET RESULT SIGN
:                   : NORMALIZE AND STORE THAT
  
```

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 F 9  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Sequence 315  
 : FLOAT .MIC [600,1204] F & D floating point : CVTBF, CVTWF, CVTLF Page 314

:11958 ;HERE FOR CONVERTS OF LONG TO FLOATING, WHICH MUST ROUND IF  
 :11959 ; THE SIGNIFICANT BITS OF INTEGER DO NOT ALL FIT IN THE FRACTION.  
 :11960  
 U 0650, F000,003F,01F0,F847,0000,0300 :11961 =00 :00-----: D.EQL.0  
 :11962 CVTLF.2:WRITE.DEST : SRC ZERO  
 :11963  
 U 0652, 0E00,183C,4180,F800,008C,A567 :11964 =10 :10-----: D.GTR.0  
 :11965 CVTLF.3:SC SC-SHF.VAL. : SRC POS: ADJUST EXP FOR NORMALIZATION  
 :11966 D BAL.NORM. : D GETS NORMALIZED FRAC  
 :11967 K[.80]. : PRESET KMX FOR SK FOR ROUNDING  
 :11968 D.BYTES?.J/CVTLF.4 : BEN ON D.NE.0, GOTO ROUNDING  
 :11969  
 U 0653, 081F,2000,0183,F800,0000,0652 :11970 :11-----: D.LSS.0  
 :11971 D 0-D. : NEGATE SOURCE  
 :11972 SB NOT.SD. : SET SIGN FLAG  
 :11973 J/CVTLF.3 : THEN NORMALIZE  
 :11974 =:END  
 :11975  
 U 0567, F808,003B,01F0,F847,0000,0300 :11976 =0111 :0-----: D<31:24>.EQL.0 (ROUNDING UNNECESSARY)  
 :11977 CVTLF.4:EALU SC,D.PACK.FP. : PREPARE RESULT  
 :11978 WRITE.DEST : STORE IT  
 :11979  
 U 056F, 0819,0014,4180,F800,0110,C915 :11980 :1-----:  
 :11981 D D+K[.80],CLK.UBCC. : ROUND THE FRAC  
 :11982 FE\_SC+1 : INC EXP TO FE IN CASE CARRY FROM ROUNDING  
 :11983 =:END  
 :11984  
 :11985  
 U 0915, 0008,0338,01C0,F800,0000,0610 :11986 EALU SC,Q.PACK.FP. : PACK RESULT FP AS IF THERE IS NO CARRY  
 :11987 C31?, J/CVTBF.1 : BEN ON ALU<C>

G 9

ZZ-ES0AA-124.0 ; FLCAT .MIC [600,1204] F & D floating point 14-Jan-82 Fiche 2 Frame 69 Sequence 316  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 315  
 : FLOAT .MIC [600,1204] F & D floating point : CVTBD, CVTWD, CVTLD

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:11988 .TOC   "      F & D floating point : CVTBD, CVTWD, CVTLD"
:11989
:11990 :      CVTB/W/LD      (6C/6D/6E)      SRC.RX, DST.WD
:11991 :ENTER HERE WITH SRC IN D
:11992
:11993 2CC: -----
:11994 CVTID: D.D.SXT[INST.DEP],Q_0,      : SIGN EXT SRC TO D
:11995 SET.CC(INST),                      : SET COND CODES
:11996 CLR.SD&SS,                        : INIT RESULT SIGN TO POSITIVE
:11997 SC_K[A0]                           : SC SET TO BIAS 128 + SHF 32
:11998
:11999 -----
:12000 RC[T1]_0,                          : ASSUME ONLY 24 BITS OF FRACTION
:12001 FE_K[8],                           : GET CONSTANT FOR RECOVERING OTHERS
:12002 SIGNS?                            : TEST FOR SRC 0, +, OR -
:12003
:12004 =00 : -----
:12005 WRITE.DEST,J/WRD                 : D.EQL.0 EASY CASE
:12006
:12007 =10 : -----
:12008 CVTID.1:D.DAL.NORM,              : NORMALIZE FRACTION
:12009 FE_SC-SHF.VAL,                  : CALCULATE EXPONENT
:12010 SC_FE,                           : GET 8 INTO SC
:12011 D.BYTES?,J/CVTID.2             : TEST BYTE 3 FOR MORE THAN 24 BITS OF FRAC
:12012
:12013 -----
:12014 D_0-D,                           : NEGATE FRACTION
:12015 SD NOT SD,                     : SET DESTINATION SIGN FLAG
:12016 J/CVTID.1                         : GO NORMALIZE AND STORE
:12017
:12018 =:END OF CONSTRAINT ON BEN/SIGNS
:12019
:12020 =0111 : -----
:12021 CVTID.2:EALU FE,D PACK.FP,       : D<31:24>.EQL.0 (RESULT FITS IN 1 LONGWORD)
:12022 WRITE.DEST                         : PACK FRAC AND EXP INTO D
:12023
:12024 -----
:12025 Q_D,                             : SAVE HIGH ORDER A MOMENT
:12026 D_DAL.SC                         : SHIFT LOW ORDER LEFT 8 PLACES
:12027
:12028 -----
:12029 RC[T1]_D.AND.K[.FF00],           : STORE LOW ORDER FRACTION BITS
:12030 D_Q,                             : GET BACK HIGH ORDER
:12031 J7CVTID.2

```

U 02CC, 0802,C03C,25FF,F800,00F4,6919

U 0919, 0003,0D3C,0180,F988,0104,6668

U 0668, F000,003F,01F0,F847,0000,0300

U 066A, 0E00,183C,0180,F800,018D,A577

U 066B, 081F,2000,0183,F800,0000,066A

U 0577, F808,003B,01F0,F847,0000,6300

U 057F, 0D00,003C,01E0,F800,0000,0920

U 0920, 0C19,0034,4D80,F988,0000,0577

H 9

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 Fiche 2 Frame H9 Sequence 317  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 316  
 : FLOAT .MIC [600,1204] F & D floating point : CVTDF, CVTDF

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:12032 .TOC   "      F & D floating point : CVTDF, CVTDF"
:12033
:12034 :CVTDF (56) SRC.RF, DST.WD
:12035 ;ENTER WITH SRC IN D.
:12036
:12037 247: -----
:12038 CVTDF: SC_D(EXP), ALU_D,      : GET EXP
:12039           SET_CC(INST),       : SET COND CODES
:12040           CHK.FLT.OPR        : CHK -0
:12041
:12042 -----
:12043 RC[T1]_K[ZERO],          : RESULT <L> IS ALWAYS 0
:12044 SC?                      : CHK FOR +0
:12045
:12046 =*01 :0-----
:12047 CVTDF.1: D_0, WRITE.DEST    : COND CODES ALREADY SHOW 0
:12048
:12049 :1-----
:12050 WRITE.DEST                 : SOURCE NON-ZERO - WRITE DEST
:12051 =;END

```

U 0247, 0001,C03C,0180,F800,08F3,0922

U 0922, 0018,1438,1980,F988,0000,03F9

U 03F9, FF00,003F,01F0,F847,0000,0300

U 03FB, F000,003F,01F0,F847,0000,0300

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204]  
; P1W124.MCR 600,1204]  
; FLOAT .MIC [600,1204]

F & D floating point 14-Jan-82  
MICRO2 1L(03) 14-Jan-82 75:30:16  
F & D floating point : CVTDF, CVTDF

I 9  
Fiche 2 Frame I9  
VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124

Sequence 318  
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U 02CD, 0019,0034,4580,F900,0010,0926

:12052 :CVTDF (76) SRC.RD, DST.WF  
:12053 :ENTER WITH SRC IN <RC 0, D>.

U 0926. 0910,0138,4185,F800,0883,04F4

:12054  
:12055 2CD:  
:12056 CVTDF: [LC RC[TO], LATCH SRC <H>  
:12057 ALU D.AND.K[.8000], CHK FOR NEED OF ROUNDING  
:12058 CLK.UBCC

U 04F4, 0819,1414,4180,F800,0110,0449

:12059  
:12060  
:12061 D.LC(FRAC), GET FRAC  
:12062 SC.LC(EXP), GET EXP  
:12063 CHR.FLT.OPR, CHK IF -0  
:12064 SS\_SS.XOR.ALU15&SD\_ALU15, SD GETS SIGN  
:12065 KE[.80], PRESET SLOW CONSTANT FOR POSSIBLE ROUNDING  
:12066 Z? HAVE TO DO ROUNDING?  
:12067  
:12068 =0 :0 YES: ROUNDING  
:12069 FE SC FE GETS OLD EXP  
:12070 D.D+K[.80], ADD 1 TO FRAC  
:12071 CLK.UBCC, HAVE TO INCREMENT EXP BY 1?  
:12072 SC?, J/CVTDF.1 CHECK FOR ZERO SOURCE

U 04F5, 0810,D438,0180,F800,0070,03F9

:12073 : \*\*\*\*\*  
:12074 : \* Patch no. 012, PCS 04F4 trapped to WCS 114C \*  
:12075 : \*\*\*\*\*  
:12076 : \*\*\*\*\*  
:12077  
:12078 :1 NO: RESULT = SRC <H>  
:12079 D.LC,SET.CC(INST). SET COND CODES  
:12080 SC?,J/CVTDF.1 CHK FOR ZERO

=;END

U 0449, FF18,C03B,19F0,F847,0070,0300

:12081  
:12082  
:12083 =\*01 :0 SOURCE WAS ZERO DESPITE RANDOM LOW BITS  
:12084 CVTDF.1: D\_0, ALU K[ZERO]. SOURCE=0 --> DEST = 0  
:12085 SET.CC(INST). SET CC'S TO REFLECT A ZERO  
:12086 WRITE.DEST AND GO STORE IT

U 0448, 0000,1B3C,0180,F800,0080,C434

:12087  
:12088 :1 POSSIBLE INCREMENT EXP  
:12089 SC SC+1, HAVE TO INCREMENT EXP?  
:12090 ALU.N?

=;END

U 0434, 0500,003C,0580,F800,0084,A43C

:12091  
:12092  
:12093  
:12094 =0\*\*\*  
:12095 CVTDF.2:  
:12096 :0 NO:  
:12097 SC SC-K[.1], GET BACK OLD EXP  
:12098 D.D.LEFT,SI/ZERO LEFT JUSTIFIED FRAC

U 043C, 0808,D438,0180,F800,0070,0601

:12099  
:12100 :1 EXP WAS INCREMENTED  
:12101 D.PACK.FP, PACK RESULT  
:12102 SET.CC(INST). SET COND CODES  
:12103 SC?,J/EXPCK CHK FOR OVERFLOW

=;END  
:12104

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 J 9  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Sequence 319  
 : FLOAT .MIC [600,1204] F & D floating point : CVTFB, CVTFW, CVTFL, CVTRFL Page 318

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;12105 .TOC   "      F & D floating point : CVTFB, CVTFW, CVTFL, CVTRFL"
;12106
;12107 : CVTFB/W/L      (48/49/4A)      SRC.RF, DST.WX
;12108 :ENTER AT B.FORK WITH SRC IN D.
;12109
;12110 245:
;12111 CVTFB: -----
;12112     D_D(FRAC),          : UNPACK FLOATING
;12113     SC_D(EXP),SS_ALU15.  : GET EXP, SIGN
;12114     CHR.FLT.OPR,        : CHECK FOR -0
;12115     CALL,J/CVTFI.O      :
;12116
;12117 255: -----
;12118 CVTFX.W:ALU.D, N AMX.Z TST,      : SET COND CODES
;12119 DT/INST.DEP, WRITE.DEST : WRITE RESULT
;12120
;12121 : ****
;12122 : * Patch no. 015, PCS 0255 trapped to WCS 1152 *
;12123 : ****
;12124
;12125
;12126 : CVTRFL      (4B)      SRC.RF, DST.WX
;12127 :ENTER AT B.FORK WITH SRC IN D.
;12128
;12129 2C1:
;12130 CVTRFL: -----
;12131     D_D(FRAC),          : SAVE INPUT, UNPACK FLOATING
;12132     SC_D(EXP),SS_ALU15.  : GET EXP, SIGN
;12133     CHR.FLT.OPR,        : CHECK FOR -0
;12134     CALL,J/CVTFI.O      :
;12135
;12136 2D1: -----
;12137     ALU.Q(A), Q_ALU.LEFT,  : RETURN FOR CVTRFL
;12138     SI/DIV, SS?          : MOVE ROUND BIT FROM Q31 TO Q00
;12139
;12140 =1110 :0-----: MOVE ROUND BIT FROM Q31 TO Q00
;12141     D_D+Q, J/CVTFX.W    : WITH Q<31-1>=0 ; TEST SIGN
;12142
;12143 :1-----: ROUND POSITIVE NUMBERS UP
;12144     D_D-Q, J/CVTFX.W    :
;12145 =END
  
```

ZZ-ESOAA-124.0 : FLOAT .MIC [600,1204]  
: P1W124.MCR 600,1204]  
: FLOAT .MIC [600,1204]

F & D floating point  
MICRO2 1L(03) 14-Jan-82 14-Jan-82 15:30:16 VAX11/780 Microcode

: F & D floating point : CVTDB, CVTDW, CVTDL, CVTRDL

K 9

Fiche 2 Frame K9

Sequence 320  
Microcode : PCS 01, FPLA OE, WCS124

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U 0243, 0010,0039,01C0,F900,0000,0680

U 0253, F001,C03F,01F0,F847,0030,0300

:12146 .TOC " F & D floating point : CVTDB, CVTDW, CVTDL, CVTRDL"  
:12147  
:12148 :CVTDB/W/L (68/69/6A) SRC.RD, DST.WX  
:12149 :ENTER AT B.FORK WITH SRC IN <RC 0, D>.  
:12150 243:  
:12151 CVTDB: -----  
:12152 Q RC[TO], : GET SRC <H>  
:12153 CALL,J/CVTDI : CALL CVT DOUBLE TO INTEGER SUBRT  
:12154  
:12155 253: -----  
:12156 ALU.D, N AMX.Z TST, : SET CONDITION CODES  
:12157 DT/INST.DEP, WRITE.DEST : WRITE RESULT  
:12158  
:12159 : \*\*\*\*\*  
:12160 : \* Patch no. 015, PCS 0253 trapped to WCS 1152 \*  
:12161 : \*\*\*\*\*

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 ; FLOAT .MIC [600,1204] F & D floating point : CVTDB, CVTDW, CVTDL, CVTRDL

L 9

Fiche 2 Frame L9

Sequence 321

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```

;12162 ;CVTRDL (6B) SRC.RD, DST.WX
;12163 ;ENTER AT B.FORK WITH SPC IN <RC 0, D>.
;12164 2C5:
;12165 CVTRDL: -----
;12166 Q_RC[T0], : GET SRC <H>
;12167 CALL,J/CVTDI : CALL CVT DOUBLE TO INTEGER SUBRT
;12168
;12169 2D5: -----
;12170 ALU_0(A), Q_ALU.LEFT, : ISOLATE ROUND BIT IN Q00
;12171 SI/DIV, SS? ; AL BY ITSELF ; TEST SIGN
;12172
;12173 =1110
;12174 CVTRDL.0: -----
;12175 :0-----: ROUND POSITIVE NUMBERS UP, SET
;12176 D_D+Q, Q_Q.RIGHT, : Q = 0
;12177 SI/ZERO, CLK.UBBC.
;12178 J/CVTRDL.1
;12179
;12180 :1-----: ROUND NEGATIVE NUMBERS DOWN, SET
;12181 D_D-C, Q_Q.RIGHT, : Q = 80000000
;12182 SI/MJL-, CLK.UBBC
;12183 =:END
;12184 CVTRDL.1: -----
;12185 Q_D.XOR.Q, Z? ; COMPARE INPUT VS RESULT SIGN
;12186 =010 :0-- : CONSTRAINT FOR Z AND Q31
;12187 Q31? ; CHECK IF INPUT AND RESULT SIGNS ARE EQUAL
;12188 =011 :01-----:
;12189 CVTRDL.2: -----
;12190 ALU_D, N_AMX.Z_TST, : SET CONDITION CODES FROM RESULT
;12191 DT/[ONG, WRITEDEST : AND GO WRITE IT
;12192
;12193 : ***** * Patch no. 015, PCS 0473 trapped to WCS 1152 *
;12194 : ***** *
;12195 : ***** *
;12196 : ***** *
;12197 : ***** *
;12198 : ***** *
;12199 : ***** *
;12200 =111 :11-----: SIGNS UNLIKE AND RESULT.NE.0 MEANS OVFLD
;12201 =:END

```

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
: P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124

M 9 Fiche 2 Frame M9 Sequence 322  
: FLOAT .MIC [600,1204] F & D floating point : CONVERT FLOATING TO INTEGER Page 321

:12203 .TOC " F & D floating point : CONVERT FLOATING TO INTEGER"

:12204  
:12205 : GENERAL UTILITY ROUTINES FOR FLOATING-TO-INTEGER CONVERSION.  
:12206 : USED BY CVTFX, CVTDX, CVTRFL, CVTRDL, EMODF, EMODD INSTRUCTIONS.

:12207 :  
:12208 : ENTRY POINTS:  
:12209 :  
:12210 : CVTFX, CVTRFL ENTER AT CVTFI.0 WITH D=UNPACKED MANTISSA,  
:12211 : SC = EXPONENT, SS = SIGN OF THE NUMBER TO CONVERT. RESERVED OPERAND  
:12212 : CHECK MUST HAVE ALREADY BEEN PERFORMED.  
:12213 : EMODF ENTERS AT CVTFI.1 WITH THE SAME PARAMETERS, EXCEPT THAT  
:12214 : THE OPERATIONS PERFORMED IN CVTFI.0 HAVE ALREADY BEEN DONE;  
:12215 : THIS IS TO AVOID LOSS OF PRECISION IN THE 32-BIT PRODUCT.  
:12216 :  
:12217 : CVTDX, CVTRDL ENTER AT CVTDI WITH PACKED DOUBLE PRECISION NUMBER  
:12218 : IN <RC 0 -- Q, D>;  
:12219 : EMODD ENTERS AT CVTFI.1 WITH LOW FRACTION IN Q  
:12220 : EXIT CONDITIONS OF THIS ROUTINE:  
:12221 :  
:12222 : EXIT IS VIA RETURN10 WITH D = INTEGER PART OF NUMBER (SIGNED),  
:12223 : Q31 = ROUND BIT (UNSIGNED), <RC[T1],RC[T2]> = MANTISSA OF  
:12224 : ORIGINAL F.P NUMBER IN NORMALIZED FORM (IF INTEGER OVERFLOWS,  
:12225 : THIS MANTISSA MAY BE SHIFTED LEFT 32 BITS OR MAY BE 0).  
:12226 : SC = AMOUNT TO SHIFT <RC[T1],RC[T2]> LEFT BY TO YIELD  
:12227 : THE FRACTIONAL PART OF THE NUMBER. SS = SIGN OF INPUT NUMBER.  
:12228 : THE CONDITION CODES N,Z, AND C ARE 0, 1 AND 0 RESPECTIVELY  
:12229 : AND V INDICATES WHETHER AN OVERFLOW HAS BEEN DETECTED  
:12230 : (OVERFLOW DETECTION IS DONE IN INSTRUCTION'S DATA TYPE)

N 9

Fiche 2 Frame N9 Sequence 323  
VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 322

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16  
; FLOAT .MIC [600,1204] F & D floating point : CONVERT FLOATING TO INTEGER

	:12231	CVTFI.0:	
	:12232		
	:12233	RC[1]_0, NZ_ALU.V&C_0, Q_0.	CLEAR MANTISSA HOLDER, SET Z
	:12234	D_D.LEFT,	CHANGE FRAC FROM UNPACKED TO NORMALIZED
	:12235	SD_SS, SC_SC-K[.80], FE_EALU	STRIP BIAS FROM EXP
	:12236	CVTFI.1:	
	:12237		
	:12238	RC[2]_Q, Q_0,	EMODF ENTERS HERE
	:12239	SC_SC-RC[.20], SC?	RC2 <- MANTISSA<L>, CLR 2 FOR RT SHIFT
	:12240		TURN EXP INTO SHIFT CT AND TEST RANGE
	:12241	=100	
	:12242	CVTFI.2:	BRANCH ON SC (RANGE OF /NUM/)
	:12243	:00-----	[CVTFI STUFF ENTERS HERE]
	:12244	Q_D, RC[1]_D, D_0,	5</NUM/<1.0 - SAVE HI MANTISSA,
	:12245	SC_FE, RETURN10	INT = 0, ROUND BIT = 1, EXIT.
	:12246	:01-----	
	:12247	RC[1]_D, D_0, Q_0,	/NUM/<.5 - SAVE HI MANTISSA,
	:12248	SC_FE, RETURN10	INT=0, ROUND=0, EXIT WITH SC<0.
	:12249	:10-----	
	:12250	RC[1]_D, Q_D, D_DAL.SC,	1</NUM/<2**31 - SAVE HI MANTISSA,
	:12251	SS?, J/CVTFI.4	D=INT, SET UP TO GET ROUND BIT,
	:12252		SEE IF WE SHOULD NEGATE INT.
	:12253	:11-----	
	:12254	Q_RC[2]	/NUM/=>2**31 - RESTORE Q FOR LEFT SHFT
	:12255		
	:12256	EALU SC, FE_EALU,	FORM MAGIC # TO
	:12257	Q_D.0XT[BYTE].OR.PACK.FP.	CHECK SPECIAL CASE (NUM=-2**31),
	:12258	D_DAL.SC, SC?	SHIFT D AS IF SC<32 & TEST IF TRUE
	:12259		
	:12260		
	:12261		
	:12262		
	:12263		
	:12264	=110	BRANCH ON SC (/NUM/ => 2**63)
	:12265	:0-----	
	:12266	ALU Q_XOR.K[.8000], CLK.UBCC,	2**31</NUM/<2**63 - SEE IF
	:12267	LC_RC[2], Q_0,	NUM=-2**31 (ONLY NON-OVERFLOW CASE)
	:12268	FE_SC, J/CVTFI.3	DECREMENT SAVED SC BY 32
	:12269		
	:12270	:1-----	
	:12271	RC[1]_LC, D_LC, Q_0.	/NUM/=>2**63 - SHIFT MANTISSA LEFT 32
	:12272	SET.V, J/CVTFI.1	LOOP UNTIL NUMBER IS SHIFTABLE
	:12273		
	:12274	CVTFI.3:	
	:12275		
	:12276	RC[1]_LC, Q_LC, SC_SC-K[.20].	CONTINUATION OF /NUM/=>2**31 CASE
	:12277	Z?	SHIFT MANTISSA LEFT 32 & ADJUST EXP
	:12278		CHECK FOR NUM=-2**31
	:12279		
	:12280	:0-----	BRANCH ON Z (NUM = 2**31)
	:12281	RC[2]_0, SET.V, SS?, J/CVTFI.4	NO - OVERFLOW - COMPLETE THE LEFT
	:12282		SHIFT AND CHECK SIGN FOR NEGATION
	:12283		
	:12284	:1-----	
	:12285	RC[2]_0, SS?, J/CVTFI.4	YES - NO OVERFLOW - COMPLETE THE LEFT
			SHIFT AND TEST FOR NEGATION

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 Fiche 2 Frame B10 Sequence 324  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 323  
 : FLOAT .MIC [600,1204] F & D floating point : CONVERT FLOATING TO INTEGER

B 10

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:12286 : FLOW CONVERGES HERE WITH D = LOW 32 BITS OF INTEGER.
:12287 : Q = MANTISSA WORD CONTAINING ROUND BIT, SC=NUMBER OF PLACES
:12288 : TO SHIFT (RIGHT) TO PUT ROUND BIT IN D$1, V SET IF OVERFLOW.
:12289 : <RC[T1],RC[T2]> CONTAINING MANTISSA SUCH THAT Q=RC[T1].
:12290 : WHAT WE HAVE TO DO IS GET THE ROUND BIT AND CHECK FOR
:12291 : DATA-TYPE OVERFLOW OF THE INTEGER.
:12292 :
:12293 :
:12294 =1110 :BRANCH ON SS (ORIGINAL NUMBER NEGATIVE)
:12295 :0-----
:12296 CVTFI.4:
:12297 RC[T3].D.SXT[INST.DEP], : CONVERT LONGWORD TO TARGET D.T.
:12298 Q_D, D_DAL.SC, J/CVTFI.5 : SAVE INT AND GET ROUND BIT
:12299 :1-----
:12300 Q_0-D, D_DAL.SC : NEGATE & SAVE INT, GET ROUND BIT
:12301 :
:12302 RC[T3].Q.SXT[INST.DEP] : CONVERT LONGWORD TO TARGET D.T.
:12303 :
:12304 CVTFI.5:
:12305 LC_RC[T3], ALU Q.XOR.LC. : CHECK FOR D.T. OVERFLOW
:12306 CLK.UBCC, D_Q, Q_D, SC_FE : D<-INT, Q<-ROUND, SC<-# BITS
:12307 :
:12308 Z? : CHECK FOR OVERFLOW (WHADDYA WASTE)
:12309 :
:12310 =0 :BRANCH ON Z (NO OVERFLOW)
:12311 :0-----
:12312 SET.V, RETURN10 : OVERFLOW - RETURN WITH V=1
:12313 :1-----
:12314 RETURN10 : NO OVERFLOW (HOWEVER V STILL MAY BE 1)
:12315 :
  
```

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : PIW124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : CONVERT FLOATING TO INTEGER

C 10

Fiche 2 Frame C10

Sequence 325

Page 324

```

:12316 : DOUBLE PRECISION ENTRY POINT
:12317
:12318 :-----;
:12319 =00 :CALL CONSTRAINT FOR UNPK
:12320 :00-----;
:12321 CVTDI: RC[T1]_0, N8Z_ALU.V&C_0, : INIT HI FRAC AND COND CODES,
:12322 SS_0&SD_0, : SET UP FOR UNPACK ROUTINE
:12323 CALL, J7UNPK : GO UNPACK DOUBLE PREC NUMBER
:12324
:12325 :01-----;
:12326 D_0, Q_0, RC[T2]_0, SC_K[ZERO], : NUMBER = 0 - ZERO WORD
:12327 RETURN10 : AND EXIT
:12328
:12329 :10-----;
:12330 D_RC[T5], Q_D, SD_SS, : GET UNPACKED MANTISSA IN <D,Q>
:12331 SC_SC-K[.80] : REMOVE BIAS FROM EXP
:12332 =:END-----;
:12333
:12334 D_D.LEFT, SI/DIVD, Q_0, : NORMALIZE MANTISSA<H> IN D, CLR Q
:12335 ALU_0+Q, RC[T2]_ALU.LEFT, : SAVE NORMALIZED MANTISSA<L> IN RC[T2]
:12336 SC_SC-K[.20], SC?, : (PSL[N]=0 SO NO GARBAGE SHIFTS IN)
:12337 J/CVTFI.2 : TURN EXP INTO SHIFT CT AND TEST RANGE
  
```

U 0680, 0003,003D,0187,F988,0050,08BE

U 0681, 0F03,003E,19F8,F990,0084,6010

U 0682, 0810,0038,41E4,F928,0084,A96E

U 096E, 053F,1414,7478,F990,0084,A4D4

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 D 10 Fiche 2 Frame D10 Sequence 326  
 : P1W124.MCR 600,1204] MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 325  
 : FLOAT .MIC [600,1204] F & D floating point : ACBF

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:12338 .TOC   "      F & D floating point : ACBF"
:12339
:12340 :GET HERE WITH LIMIT OPERAND IN Q, ADDEND IN D
:12341
:12342 3C5: -----
:12343 ACBF: R[R15] D.                                :SAVE ADDEND (SRC)
:12344 D D(FRAC),SC_D(EXP).                         :UNPACK ADDEND
:12345 SS_ALU15.                                     :SETUP SRC SIGN FLAG
:12346 STATE_K[ZERO],CLK.UBCC                      :CLEAR STATE AND EALU CC
:12347
:12348 =0***00100:-----:CALL SITE FOR GETTING INDEX
:12349   RC[T3] Q.                                    :SAVE LIMIT
:12350   CHK.FLT.OPR.                               :PROTECT AGAINST RESERVED OPERAND
:12351   IDET2] D.                                   :SAVE ADDEND FRAC WHILE GETTING BDEST
:12352   CALL.J7SPEC                                :GO GET INDEX OPERAND
:12353
:12354 =0***10100:-----:RETURN HERE WITH MEMORY OPERAND
:12355   STATE_K[.]                                 :FLAG INDEX AS MEMORY OPERAND
:12356
:12357 =0***10110:-----:RETURN HERE WITH REGISTER OPERAND
:12358   RC[T0] D.                                    :SAVE INDEX (DST) OPERAND
:12359   D D(FRAC),FE_D(EXP).                         :UNPACK INDEX OPERAND
:12360   CRK,FLT.OPR,CLK.UBCC.                      :CHECK RESERVED OPERAND
:12361   SS_SS.XOR.ALU15&SD_ALU15.                  :SETUP OP SELECT AND DEST SIGN
:12362   Q_IB.BDEST,PC_PC+2.                         :GET BRANCH DISPLACEMENT FROM IB
:12363   CALL,IB.TEST?.J/ACBF.3
:12364
:12365 =1***10110:-----:RETURN HERE IF ADD UNNECESSARY
:12366   ALU_D.XOR.R[R15].SS_ALU15.                 :SET SS TO DIFF OF INDEX & ADDEND SIGNS
:12367   SC_R[ZERO].                                :CLEAR OVERFLOW FLAG
:12368   STATE0?.J/ACBF.5                           :TEST WHERE TO STORE INDEX
:12369
:12370 : *****
:12371 : * Patch no. 009, PCS 05B6 trapped to WCS 1149 *
:12372 : *****
:12373
:12374 =1***11110:-----:NORMAL COMPLETION OF FLOATING ADD
:12375 ACBF.2: EALU_SC,D_PACK.FP.                   :REBUILD FLOATING RESULT
:12376   SET_CC(INST).                            :SET CONDITION CODES ON IT
:12377   SC?.J/ACBF.4                            :GO TEST FOR OVER/UNDERFLOW
:12378
:12379 =1***11111:-----:ROUNDING CAUSED DENORMALIZATION
:12380   D_D.RIGHT,                                :RESTORE NORMALIZATION OF FRACTION
:12381   ST_SC+1,J/ACBF.2                          :GO PACK UP RESULT
  
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ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 E 10  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : ACBF Fiche 2 Frame E10 Sequence 327  
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:12382 ;HERE IN ACB FLOATING, TO GET THE BRANCH DESTINATION AND BEGIN THE ADD  
 :12383  
 U 0698. 0000.003D.0180.F800.0000.0E6E :12384 =00 :-----;TB MISS  
 :12385 ACBF.3: CALL.J/IB.TBR ;TB REFILL REQUIRED  
 :12386  
 U 0699. 0000.003D.0180.F800.0000.0880 :12387 :-----;ERROR  
 :12388 CALL.J/IB.ERR  
 :12389  
 U 069A. 7000.0B3C.01F0.F800.0000.0698 :12390 :-----;STALL  
 :12391 Q\_IB.BDEST ;TRY AGAIN TO GET BRANCH DISPLACEMENT  
 :12392 IB.TEST?,J/ACBF.3 ;LOOP UNTIL IT COMES  
 :12393  
 U 069B. D015.3214.C9F0.2DB8.0090.E689 :12394 :-----;GOT IT  
 :12395 RCE[7].Q+PC,  
 :12396 CLR.IB.SPEC,  
 :12397 Q\_ID[T2],  
 :12398 ST\_NABS(SC-FE),CLK.UBCC.  
 :12399 EALU?  
 :12400 :-----;CALCULATE EXPONENT DIFFERENCE  
 :12401 =;END OF CONSTRAINT FOR IB.TEST ;CHECK EXPONENTS FOR ZERO  
 :12402  
 U 0689. D000.003C.0180.FA78.0800.0972 :12403 =1001 :-----;EALU Z=0, SC.EQL.0  
 :12404 ALU\_R[R15],CHK.FLT.OPR. ;ADDEND EXP IS ZERO. RESERVED OPERAND?  
 :12405 CLR.IB.SPEC,  
 :12406 J/ACBF.3A ;CLEAR 2ND BYTE OF BDEST  
 :12407 ; IF NOT, RETURN INDEX AS SUM  
 :12408 :-----;EALU Z=0, SC.NEQ.0  
 :12409 ID[T1].D,  
 :12410 CLR.IB.SPEC,  
 :12411 EALU?,J/ADDFSH ;SAVE INDEX FRACTION,  
 :12412 :-----;CLEAR 2ND BYTE OF BDEST  
 :12413 D\_0,  
 :12414 ALU\_R[R15],CHK.FLT.OPR. ;GO ADD FLOATING  
 :12415 CLR.IB.SPEC,  
 :12416 RETURN100 ;BOTH ZERO, SUM IS ZERO  
 :12417 :-----;BEWARE RESERVED OPERAND  
 :12418 :-----;CLEAR 2ND BYTE OF BDEST  
 :12419 :-----;EALU Z=1, SC.EQL.0  
 :12420 D\_R[R15],  
 :12421 CLR.IB.SPEC, ;INDEX IS ZERO, RETURN ADDEND AS SUM  
 :12422 RETURN100 ;CLEAR 2ND BYTE OF BDEST  
 :12423  
 U 068F. D800.003E.0180.FA78.0000.0100 :12424 =;END OF CONSTRAINT FOR EXPONENT TEST  
 :12425  
 :12426  
 :12427 ACBF.3A:D RC[T0],  
 :12428 RETURN100 ;ADDEND IS ZERO, RETURN INDEX UNCHANGED

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204]  
; P1W124.MCR 600,1204]  
; FLOAT .MIC [600,1204]

F & D floating point  
MICR02 1L(03) 14-Jan-82 14-Jan-82 15:30:16  
F & D floating point : ACBF

F 10

14-Jan-82

15:30:16

VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124

Fiche 2 Frame F10

Sequence 328

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U 0691, 0818,039,1980,F800,00F4,6E09

:12429 ;HERE IN ACBF, TO CHECK FOR UNDER/OVERFLOW OF EXPONENT  
:12430  
:12431 =0001 :0001-----;SC.EQL.O  
:12432 ACBF.4: D\_K[ZERO],SET.CC(INST), ;RETURN ZERO ON UNDERFLOW  
:12433 ST\_K[ZERO], ;CLEAR OVERFLOW FLAG  
:12434 CALL,J/UNDRFL  
:12435

U 0693, 000D,1720,1981,FA78,0084,6598

:12436 FL.PA.9:;0011-----;1.LEQ.SC.LEQ.FF  
:12437 ALU\_D.XOR.R[R15].SS\_ALU15, ;DIFF OF ADDEND & INDEX SIGNS TO SS  
:12438 SC\_R[ZERO], ;CLEAR OVERFLOW FLAG  
:12439 STATE0?,J/ACBF.5 ;WHERE IS RESULT STORED?  
:12440

U 0695, 0818,039,1980,F800,00F4,6E09

:12441 :0101-----;SC.LSS.O  
:12442 D\_K[ZERO],SET.CC(INST), ;RETURN ZERO ON UNDERFLOW  
:12443 ST\_K[ZERO], ;CLEAR OVERFLOW FLAG  
:12444 CALL,J/UNDRFL  
:12445

U 0697, 0818,039,4580,F800,0070,0E03

:12446 :0111-----;SC.GTR.FF  
:12447 D\_K[.8000],SET.CC(INST), ;RETURN RESERVED OP ON OVERFLOW  
:12448 CALL,J/OVFL  
:12449

U 069F, 0000,173C,0181,FA78,0000,0598

:12450 =1111 :1111-----;RETURN AFTER OVER/UNDERFLOW  
:12451 ALU\_R[R15].SS\_ALU15, ;ADDEND SIGN TO SS  
:12452 STATE0?  
:12453

=;END OF CONSTRAINT FOR OVER/UNDERFLOW TEST

:12455  
:12456 =0-----;INDEX IS IN REGISTER  
:12457 ACBF.5: R(PRN) D\_LONG, ;STORE RESULT  
:12458 Q\_D,STATE\_K[.1], ;SET "SINGLE" FLAG  
:12459 PSL.V?,J/ACBF.6

U 0598, 0001,1A3C,05E0,F8D8,1404,659D

:12460  
:12461 -----;INDEX IN MEMORY  
:12462 CACHE\_D[INST.DEP], ;STORE IT  
:12463 Q\_D,STATE\_K[.1], ;SET "SINGLE" FLAG  
:12464 PSL.V?,J/ACBF.6

U 0599, 0000,DA3C,05E0,3000,1404,659D

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 G 10  
 ; P1W124.MCR 600,1204] MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Sequence 329  
 ; FLOAT .MIC [600,1204] F & D floating point : ACBF Page 328

U 059D, 0811.6020,0584,F918,0114,6974

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:12465 :HERE FOR ACBF OR ACBD AFTER STORING UPDATED INDEX.
:12466
:12467 =1101 :-----;PSL.V =0
:12468 ACBF.6: D.Q.XOR.RC[T3], :GET DIFFERENCE BETWEEN INDEX AND LIMIT
:12469 WORD,CLK,UBCC. :TESTING ONLY SIGN, EXP, AND MSB'S
:12470 SD SS, :COPY XOR OF ADDEND & INDEX SIGNS TO SD
:12471 FE_K[.1], :CLEAR EALU CC'S
:12472 J/A:BF.6A
:12473
:12474 : ****
:12475 : * Patch no. 001, PCS 059D trapped to WCS 1140 *
:12476 : ****
:12477
:12478 :-----;PSL.V =1
:12479 CLR.IB.OPC,PC_PC+1,J/IRD ;DO NOT BRANCH
:12480
:12481
:12482 ACBF.6A:D.D.OXT[WORD].XOR.Q, :NOW D<31:16>=INDEX, D<15:0>=LIMIT<15:0>
:12483 ALU?
:12484
:12485 =0011 :-----;ALU N&Z=0 (SIGNS SAME, MAGN DIFFER)
:12486 ALU_Q,XOR,D,CLK,UBCC ;COMPARE INDEX MAGNITUDE TO LIMIT
:12487
:12488 :-----;ALU Z=1 (BITS 15:0 EQUAL)
:12489 ALU_Q,XOR,LC,LONG,CLK,UBCC, ;SET Z IF EQUAL IN 32 BITS
:12490 EALU_FE, ;KEEP EALU CC CLEAR
:12491 SD NOT.SD, ;SD=1 IFF ADDEND SIGN = INDEX SIGN
:12492 Q_ID[T6], ;GET LIMIT<L> IN CASE ACBD
:12493 C31?,J/ACBF.8 ;TEST MAGNITUDE COMPARE
:12494
:12495 :-----;ALU N=1 (SIGNS DIFFER)
:12496 CLR.IB.OPC,PC_PC+1. ;TEST ADDEND SIGN .XOR. INDEX SIGN
:12497 EALU?
:12498
:12499 =:END OF ALU N&Z CONSTRAINT
:12500
:12501 =0 :-----;SS =0 DO NOT BRANCH
:12502 ACBF.7: IRD
:12503
:12504
:12505 :-----;SS =1 BRANCH
PC&VA_RC[T7],FLUSH.IB,J/IB.FILL
  
```

U 059F, C000.003C,0180,F804,4000,0062

U 0974, 081F,5B20,0180,F800,0000,06A3

U 06A3, 001D,2020,018C,F800,0010,06A7

U 06A7, 0011,2320,D9F3,2C00,0010,6680

U 06AB, C000,123C,0180,F804,4000,05A4

U 05A4, F80C,0038,01F1,F857,139B,6000

U 05A5, 2010,0038,0180,F939,4200,00AB

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;12506 ;HERE IN ACBF/D FOR COMPARE OF INDEX TO LIMIT.
;12507 ; WHEN BITS <15:0> OF INDEX AND LIMIT ARE EQUAL.
;12508
;12509 =00 ;-----;ALU C=0 (INDEX .EQ, LIMIT)
;12510 ACBF.8: SS_SD, ;GET SS= ADDEND SIGN.EQV, INDEX SIGN
;12511 D_Q,XOR,RC[T1], ;COMPARE LIMIT<L> TO INDEX<L>
;12512 WORD,CLK,UBCC,EALU_FE,
;12513 Z? ;IF EQUAL, ALWAYS BRANCH
;12514
;12515 =10 ;-----;ALU C=1 OR Z=0
;12516 CLR,IB,OPC,PC,PC+1,
;12517 EALU?,J/ACBF.7
;12518
;12519 =11 ;-----;Z=1 (^INDEX .EQ, LIMIT)
;12520 D_D,0XT[WORD].XOR.Q, ;D<31:16>=LIMIT, D<15:0>=INDEX
;12521 STATE0? ;HAVE WE COMPARED FULL OPERANDS?
;12522
;12523 =0 ;-----;STATE 0=0, MUST COMPARE LOW OF DOUBLE
;12524 ALU Q,XOR,D,CLK,UBCC,LONG, ;COMPARE LIMIT<47:32> WITH INDEX
;12525 EALU FE, ;KEEP EALU CC'S CLEAR
;12526 SD_NOT,SD, ;SD= ADDEND SIGN.XOR.INDEX SIGN
;12527 ALU?,J/ACBF.10
;12528
;12529 ;-----;STATE 0=1. INDEX .EQ. LIMIT
;12530 PC&VA_RC[T7],FLUSH,IB,J/IB,FILL ;BRANCH
;12531
;12532
;12533 =1010 ;-----;ALU Z =0
;12534 ACBF.10:C31?,J/ACBF.8 ;LIMIT<47:32> .NEQ. INDEX<47:32>
;12535
;12536 ;-----;ALU Z =0
;12537 C31?,J/ACBF.8
;12538
;12539 ;-----;ALU Z =1, C31 =0 (LIMIT.LSS.INDEX)
;12540 SS_SD ;INVERT BRANCH SENSE YET AGAIN
;12541
;12542 ;-----;ALU Z =1, C31 =1 (LIMIT.GTR.INDEX)
;12543 CLR,IB,OPC,PC,PC+1,
;12544 EALU?,J/ACBF.7
  
```

I 10

Fiche 2 Frame I10      Sequence 331  
VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124      Page 330

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204]      F & D floating point 14-Jan-82  
P1W124.MCR 600,1204]      MICRO2 1L(03)      14-Jan-82 15:30:16

; FLOAT .MIC [600,1204]      F & D floating point : ACBD

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:12545 .TOC   "      F & D floating point : ACBD"
:12546
:12547 ;HERE WITH LIMIT<H> IN RC[T0], LIMIT<L> IN Q,
:12548 ; ADDEND<H> IN RC[T1], AND ADDEND<L> IN D
:12549
:12550 384: -----
:12551 ACBD:  RC[T6]_D(B),          ;SAVE ADDEND<L> FOR UNPACK
:12552      D_Q,                   ;READY TO SAVE LIMIT<L>
:12553      ST_O(A),CLK,UBCC,     ;INIT FOR EALU BRANCH
:12554      STATE_O(A)           ;INIT STATE
:12555
:12556 -----
:12557      ID[T6]_D,             ;SAVE LIMIT<L> TOO
:12558      D_RC[T0],            ;READY TO SAVE LIMIT<H>
:12559      INTRPT,STROBE
:12560
:12561 =10****0: -----;CALL SITE FOR GETTING INDEX
:12562      ID[T5]_D,             ;SAVE LIMIT<H>
:12563      ALU_RC[T1],SS_ALU15,  ;GET ADDEND SIGN TO SS
:12564      CALC,INTERRUPT.REQ?,J/ASPC ;GO GET INDEX ADDRESS
:12565
:12566 =11****0: -----;RETURN HERE WITH MEMORY OPERAND
:12567      ID[T7]_D,             ;SAVE ADDRESS OF INDEX
:12568      J/ACBD.2              ;THEN GO GET INDEX
:12569
:12570 =11****1: -----;HERE WITH REGISTER OPERAND
:12571      RC[T0]_D               ;SAVE INDEX<H>
:12572
:12573 -----
:12574      D_R(PRN+1),           ;GET INDEX<L>
:12575      EALU?,J/ACBD.4        ;TEST ADDEND SIGN
:12576
:12577 ;HERE WHEN INDEX IS IN MEMORY. ADDRESS HAS BEEN SAVED IN ID[T7]
:12578
:12579
:12580 ACBD.2: D_CACHE,INST,DEP,    ;GET INDEX<H>
:12581      STATE_K[.10]           ;SET MEMORY OPERAND FLAG
:12582
:12583
:12584      RC[T0]_D,             ;SAVE INDEX<H> WHERE UNPACK WILL FIND IT
:12585      VA_VA+4               ;GET ADDRESS FOR INDEX<L>
:12586
:12587
:12588      D[LONG]_CACHE,         ;GET INDEX<L>
:12589      EALU?,J/ACBD.4        ;TEST ADDEND SIGN

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ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 J 10  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : ACBD Fiche 2 Frame J10 Sequence 332  
 Page 331

;12590 ;HERE IN ACBD WITH INDEX<L> IN D, BRANCHING ON ADDEND SIGN  
 ;12591  
 ;12592 =1\*0 :----- ;SS =0 (ADDEND IS POSITIVE)  
 ;12593 ACBD.4: RC[T3] D, ;SAVE INDEX<L> FOR UNPACK ROUTINE  
 ;12594 Q IB.BDEST,PC PC+1, ;GET BRANCH DISPLACEMENT  
 ;12595 IB.TEST?,J/ACBD.5 ;WAIT UNTIL IT ARRIVES  
 ;12596  
 ;12597 :----- ;SS =1 (ADDEND IS NEGATIVE)  
 ;12598 STATE STATE.OR.K[.20], ;REMEMBER THAT  
 ;12599 RC[T3] D, ;SAVE INDEX<L> FOR UNPACK ROUTINE  
 ;12600 Q IB.BDEST,PC PC+1, ;GET BRANCH DISPLACEMENT  
 ;12601 IB.TEST?,J/ACBD.5 ;WAIT UNTIL IT ARRIVES  
 ;12602  
 ;12603 =00 ACBD.5: CALL,J/IB.TBM ;REFILL TB  
 ;12604  
 ;12605  
 ;12606 :----- ;SERVE ERROR  
 ;12607 CALL,J/IB.ERR  
 ;12608  
 ;12609 :----- ;STALL  
 ;12610 Q\_IB.BDEST,IB.TEST?,J/ACBD.5 ;WAIT FOR BDEST TO ARRIVE  
 ;12611  
 ;12612 :----- ;GOT IT  
 ;12613 RC[T7] Q+PC, ;CALCULATE BRANCH ADDRESS  
 ;12614 CLR.IB.SPEC.  
 ;12615 Q D,  
 ;12616 SC\_K[.10] ;CLEAR 1ST BYTE OF BDEST  
 ;12617 ;COPY INDEX<L> FOR SWAP  
 ;12618 ;SETUP SC FOR SWAP OF HALVES  
 ;12619 :\*\*\*\*\*  
 ;12620 : \* Patch no. 003, PCS 06C3 trapped to WCS 1142 \*  
 ;12621 :\*\*\*\*\*  
 ;12622 =0\*\*00 :----- ;CALL SITE FOR UNPACK  
 ;12623 D DAL.SC, ;SWAP HALVES OF INDEX<L>  
 ;12624 SC\_K[.FFF9], ;GET -7 FOR SHIFT  
 ;12625 CLR.IB.SPEC,CALL,J/UNPACK ;CLEAR 2ND BYTE OF BDEST  
 ;12626  
 ;12627 :----- ;SRC.EQL. 0  
 ;12628 Q\_ID[T7], ;GET ADDRESS OF INDEX IF MEMORY  
 ;12629 LT RC[T1] ;GET INDEX<L> TO LATCH  
 ;12630 STATE4?,J/ACBD.6 ;WHERE SHOULD RESULT BE STORED?  
 ;12631  
 ;12632 :----- ;DST.EQL. 0  
 ;12633 Q\_ID[T7], ;GET ADDRESS OF INDEX IF MEMORY  
 ;12634 LT RC[T1] ;GET INDEX<L> TO LATCH  
 ;12635 STATE4?,J/ACBD.6 ;WHERE SHOULD RESULT BE STORED?  
 ;12636  
 ;12637 :----- ;NEITHER ZERO  
 ;12638 FE\_NABS(SC-LA(EXP)), ;CALCULATE SHIFT AMOUNT  
 ;12639 CLR.UBCC,CALL,J/ADDD.6 ;NOTE ITS DIRECTION, GO FINISH THE ADD  
 ;12640  
 ;12641 =1\*\*11 :----- ;RETURN FROM ADDD/PACKD  
 ;12642 Q\_ID[T7], ;GET ADDRESS OF INDEX IF MEMORY  
 ;12643 LT RC[T1] ;GET INDEX<L> TO LATCH  
 ;12644 STATE4?,J/ACBD.6 ;WHERE SHOULD RESULT BE STORED?

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 K 10  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : ACBD Fiche 2 Frame K10 Sequence 333  
 Page 332

	:12645	;HERE IN ACBD TO STORE INDEX	
	:12646		
	:12647	=10	;STATE 4=0 (INDEX IN REGISTER)
	:12648	ACBD.6: R(PRN)_D,SS_ALU15.	;STORE INDEX<H>, SET SS FROM SIGN
	:12649	ID[T0]_D.	;SAVE INDEX<H> WHILE <L> BEING STORED
	:12650	J/ACBD.7	;TEST FOR NEGATIVE ADDEND
	:12651		
	:12652		;STATE 4=1 (INDEX IN MEMORY)
U 06D2. 0001.003C.C181.3CD8.0000.0982	:12653	VA_Q	;RELOAD ADDRESS OF INDEX
	:12654	ID[T0]_D	;SAVE INDEX<H> DURING STORE
	:12655		
	:12656		
U 097E. 0001.C03C.0181.3000.0000.0980	:12657	CACHE_D[INST_DEP].	;STORE INDEX<H>
	:12658	ALU_D,SS_ALU15	;SET SS FROM SIGN OF INDEX
	:12659		
	:12660		
U 0980. 0810.0038.D5F0.2C03.0000.0981	:12661	VA_VA+4.	;ADVANCE ADDRESS TO INDEX<L>
	:12662	D_C	;GET INDEX<L> FROM LATCH
	:12663	Q_ID[T5]	;GET LIMIT<H> FOR COMPARE
	:12664		
	:12665		
U 0981. 0000.163C.0180.3000.0000.04E1	:12666	CACHE_D[LONG],	;STORE INDEX<L>
	:12667	STATE5?,J/ACBD.8	
	:12668		
	:12669		
U 0982. 0010.1638.D5F0.2CE0.0000.04E1	:12670	ACBD.7: R(PRN+1)_LC.	;STORE INDEX<L>
	:12671	Q_ID[T5].	;GET LIMIT<H> FOR COMPARE
	:12672	STATE5?	;TEST FOR NEGATIVE ADDEND
	:12673		
	:12674		;STATE 5=0. (ADDEND IS POSITIVE)
U 04E1. 0001.3A3C.C1F0.2D98.0000.059D	:12675	ACBD.8: RC[T3]_Q,	;PUT LIMIT WHERE ACBF WANTS IT
	:12676	Q_ID[T0].	;GET INDEX TOO
	:12677	PSL.V?,J/ACBF.6	;GO COMPARE THEM
	:12678		
	:12679		;STATE 5=1. (ADDEND IS NEGATIVE)
	:12680	ALU_K[.8000].	;SET ALU15
	:12681	SS_SS_XOR_ALU15&SD_ALU15.	;COMPLEMENT INDEX SIGN IN SS
U 04E3. 0018.0038.4585.F800.0000.04E1	:12682	J/ACBD.8	

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 L 10  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 Fiche 2 Frame L10 Sequence 334  
 ; FLOAT .MIC [600,1204] F & D floating point : MULD VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 333

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:12683 .TOC   "      F & D floating point : MULD"
:12684
:12685 .FFLIST ;Re-enable full listing
:12686 .REGION/<WCSR1L>,<WCSR1H>/<WCSR2L>,<WCSR2H>
:12687
:12688 :DOUBLE FLOATING POINT ARITHMETIC MULD ROUTINE.
:12689
:12690 :USED BY POLYD AND EMOOD AS WELL AS BY MULD
:12691
:12692 :THIS ROUTINE MULTIPLIES A 56-BIT 'DST' BY A 64 BIT 'SRC'
:12693 :TO PRODUCE A PRODUCT WITH 63 OR 64 SIGNIFICANT BITS, DEPENDING
:12694 :ON THE MAGNITUDE OF THE INPUT FRACTIONS.
:12695
:12696 :THE 'DST' IS IN <RC1,D>; THE 'SRC' IN <RC0,Q>
:12697
:12698 :WHEN CALLED BY MULD OR POLYD, THE SRC REALLY HAS ONLY 56 SIGNIFICANT BITS.
:12699
:12700 :THIS ROUTINE RETURNS 10 IF THE PRODUCT IS ZERO WITH D=Q=RC[T1]=SC=0.
:12701 :IF THE PRODUCT IS NON-ZERO AND IT WAS CALLED FROM POLY OR EMOD
:12702 :IT RETURNS 12 OR 13 WITH THE UNNORMALIZED PRODUCT IN <D,Q>, DEPENDING
:12703 :ON HOW MANY LEADING ZERO BITS ARE IN THE PRODUCT.
:12704 :SS AND SD BOTH HAVE THE RESULT SIGN
:12705 :IF THE PRODUCT IS NON-ZERO AND IT WAS CALLED FROM MULD IT RETURNS
:12706 :THE PACKED RESULT IN <D,RC[T1]>.
:12707 :OVERFLOW/UNDERFLOW CHECKING IS ONLY DONE ON THE MULD PATH.
:12708
:12709
:12710 1003: ;ASSIGN THIS ADDRESS BECAUSE PCS CALLS IT
:12711 MULD.00:-----+
:12712     RC[T6],D, D_Q,          : SAVE DST0 <L>, D GETS SRC0<L>
:12713     SC_K[.T0]             : SC GETS 16. FOR SWAP WORD OF FRAC <L>
:12714
:12715 =00 :00-----+
:12716 MULD.02:RC[T3],D, D_DAL.SC, : SAVE SRC0 <L>, SWAP WORDS OF SRC0<L>
:12717     SC_K[.FFF9],           : SETUP SHIFT AMOUNT -7
:12718     CALL,J/UNPACK         : CALL UNPACK DOUBLE FLOATING PT OPERANDS ROUTINE
:12719
:12720     :01-----+
:12721     RC[T1],_0,D,_0,Q,_0,  : RETURN1, SRC = 0, DST MAY BE 0
:12722     SC_ALU,_FE_K[.T0],    : RESULT IS 0
:12723     N8Z_ALU,V&C,_0,       : CLR EXP FOR POLYD, SET FF FOR EMOOD
:12724     RETURN10               : SET CC'S, GOTO SET WRITE RESULT READY
:12725
:12726     :10-----+
:12727     RC[T1],_0,D,_0,Q,_0,  : RETURN2, SRC.NE.0, DST = 0
:12728     SC_ALU,_FE_K[.T0],    : RESULT IS 0
:12729     N8Z_ALU,V&C,_0,       : CLR EXP FOR POLYD, SET FE FOR EMOOD
:12730     RETURN10               : SET CC'S, GOTO SET WRITE RESULT READY
:12731
:12732     :11-----+
:12733     RC[T2],D,              : RETURN3, SRC.NE.0, DST.NE.0
:12734     D.D.RIGHT,SI/ZERO,    : SAVE DST FRAC <L>, SET AS MULT'CAND*2
:12735     SC_FE,                : DST FRAC <L>/2 AS MULT'CAND
:12736     SD_SS, STATE1?        : SC GETS DST(EXP) - SRC(EXP)
:12737                         : SET RESULT SIGN TO SD & CHECK IF EMOOD
:12738 =;END
  
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U 1003, 0C01,003C,6580,F980,0084,72C8  
 U 12C8, 0D01,003D,BD80,F998,0084,66CA  
 U 12C9, 0F03,003E,65F8,F988,01D6,6010  
 U 12CA, 0F03,003E,65F8,F988,01D6,6010  
 U 12CB, 0601,173C,0184,F990,0081,12A9

ZZ-ESOAA-124.0 : FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 M 10  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : MULD Fiche 2 Frame M10 Sequence 335  
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U 12A9, 0C01.003C.41F8,FAF8,0114.B108	:12736 : AT THIS POINT,	
	:12737 : ID[T0]=SRC<H> ID[T1]=DST<H> ID[T2]=SRC<L>	
	:12738 : RC[T2]=DST<L> RC[T5]=DST<H> D =DST<L>/2 Q =SRC<L>	
	:12739 :	
	:12740 :	
	:12741 =**01 :BRANCH ON STATE<1> (EMODD)	
	:12742 :0----- MULD (OR POLYD)	
	:12743 :R[R15]_D,CLK.UBCC, MULT'CAND TO R15	
	:12744 :D_Q, Q_Q, MULTIPLIER TO D	
	:12745 :FE_SC-R[E.80], J/MULD.03 : ADD EXP BIAS 128. TO TEMP EXP RESULT	
	:12746 :	
	:12747 :1----- EMODD - MUST ADD EXTENSION TO SRC FRACT	
	:12748 :Q_ID[T0], D_Q, SRC<H> IN Q, SRC<L> IN D	
	:12749 :R[R15]_D, CLK.UBCC : SAVE DST<L> WHILE WE PAD OUT SRC	
	:12750 :	
	:12751 :D_D.LEFT, Q_Q.LEFT SHIFT SRC FRACT LEFT	
	:12752 :SI/ASHL, FE_SC-K[E.80] REMOVE EXTRA EXP BIAS	
	:12753 :	
	:12754 :D_D.OR.RC[T4] : PUT SRC EXTENDER AT LOW END OF FRACT	
	:12755 :	
	:12756 :ID[T2]_D, D_Q, Q_D : SAVE EXTENDED SRC IN ITS OLD SPOT	
	:12757 :	
	:12758 :ID[T0]_D, D_Q, Q_O : FINISH SAVING SRC AND PREPARE TO MULTIPLY	
	:12759 :	
	:12760 :	
	:12761 :	
	:12762 :ID[T0]_D, D_Q, Q_O : MULD.03 :0----- DST <L> TIMES SRC <L>	
	:12763 :=0* MULD.03: LC_RC[T2]. LATCH M'CAND * 2	
	:12764 :SC_R[E.F]. SET LOOP CT FOR 16. LOOPS	
	:12765 :CALL. Z?, J/MULDMPY GOTO MULTIPLICATION SETUP	
	:12766 :	
	:12767 :	
	:12768 :	
	:12769 :	
	:12770 :	
	:12771 :ALU_D, N_AMX_Z_TST. RETURN FROM MUL SUBRT	
	:12772 :D_Q, Q_ID[T0]. PRODUCT IS 1 PLACE TOO FAR RIGHT. SINCE WE	
	:12773 :LC_RC[T2] HALVED THE LOW DEST FRACT BEFORE MULTIPLYING:	
	:12774 :=END : THEREFORE SAVE THE 32ND BIT IN PSL<N>. D GETS PROD<H>, BRING SRC<H> INTO Q.	
	:12775 :	
	:12776 :=0* :0----- DST <L> TIMES SRC <H>	
	:12777 :D_Q, Q_D, SC_K[E.F]. IMMEDIATE PROD TO Q, MULT'IER TO D	
	:12778 :CALL. Z?, J/MULDMPY GOTO MULTIPLICATION SETUP	
	:12779 :	
	:12780 :	
	:12781 :D_Q, Q_D, LC_RC[T5] : RETURN FROM MULTIPLY SUBROUTINE	
	:12782 :	
	:12783 :	
	:12784 :	
	:12785 :ALU_Q, RC[T6]_ALU.LEFT. SHIFT THE QUANTITY <D, Q, PSL<N>> LEFT 1 PLACE	
	:12786 :D_D.LEFT, SI/DIVD TO FORM THE HIGH 64-BITS OF DST<L> X SRC	
	:12787 :	
	:12788 :	
	:12789 :R[R15]_LC, ID[T3]_D, Q_LC : IN <D, RC6>	
	:12790 :	

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204]  
; P1W124.MCR 600,1204]  
; FLOAT .MIC [600,1204]

F & D floating point 14-Jan-82  
MICR02 1L(03) 14-Jan-82 15:30:16

F & D floating point : MULD

N 10

14-Jan-82

VAX11/780

Microcode

: PCS 01, FPLA 0E, WCS124

Fiche 2 Frame N10

Sequence 336

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U 1392. 0021,203C,C9F0,2D80,0000,1118

;12791  
;12792  
;12793 RC[T0] Q.LEFT,SI/ZERO, ; GET 2 TIMES M'CAND  
;12794 Q\_ID[T2] ; GET SRC FRAC <L>

U 1118. 0C00,003D,61F8,F900,0084,70E8

;12795 =0\* ;0----- DST <H> TIMES SRC <L> PLUS (DST<L> X SRC)<L>  
;12796 D\_Q, Q\_0, SC\_K[E.F], D GETS MULT'IER, Q GETS 0(CAN'T ADD - OVFL)  
;12797 LCT RC[T0], LATCH 2 TIMES M'CAND  
;12798 CALL, J/MULDMPY GOTO SETUP MULTIPLICATION

U 111A. 0811,0014,0180,F800,0010,1394

;12799  
;12800 ;1----- RETURN FROM MUL SUBRT  
;12801 D\_D+LC, CLK.UBCC ADD (DST<L> X SRC)<L> TO (DST<H> X SRC<L>)<L>  
;12802 ;1----- (LC CONTAINS RC[T6] FROM MULDMPY)

U 1394. 0C01,033C,CDF0,2C00,0030,111C

;12803 =;END  
;12804  
;12805 ;-----  
;12806 ALU\_D, N AMX.Z\_TST, SAVE CURRENT SUM<L><31> IN PSL<N>  
;12807 D\_Q, Q\_ID[T3], C31? SET UP FOR HIGH-ORDER ADD

U 111C. 001D,0014,C1F0,2DB0,0010,1130

;12808  
;12809 =0\* ;0----- NO CARRY - ADD, SAVE RESULT ACROSS FINAL MPY  
;12810 ALU\_D+Q, RC[T6]\_ALU, SAVE THE CARRY IF THERE IS ONE  
;12811 CLK.UBCC,  
;12812 Q\_ID[T0], J/MULD.04 LOAD SRC<H> FOR FINAL MULTIPLY

U 111E. 001D,0010,C1F0,2DB0,0010,1130

;12813  
;12814 ;1-----  
;12815 ALU\_D+Q+1, RC[T6]\_ALU, CARRY - ADD WITH CARRY, SAVE RESULT,  
;12816 CLK.UBCC, SAVE THIS CARRY IF THERE IS ONE  
;12817 Q\_ID[T0] Q = SRC<H> FOR LAST MULTIPLY

=;END

U 1130. 0C00,003D,61F8,F900,0084,70E8

;12818  
;12819  
;12820 =0\* ;0----- FRAC <H> TIMES FRAC <H>  
;12821 MULD.04: LC\_RC[T0], RE-LATCH 2 TIMES M'CAND  
;12822 D\_Q, Q\_0,  
;12823 SC\_K[E.F], MULT'IER <H> TO D, Q = 0 (OVFL PROBLEMS)  
;12824 CALL, J/MULDMPY SETUP LOOP CT  
;12825 ;1----- GOTO SETUP MULTIPLICATION

U 1132. 0C11,0314,01C0,F800,0010,1134

;12826 ;1----- RETURN FROM MUL SUBRT  
;12827 Q\_D+LC, CLK.UBCC, D\_Q, SWAP HALVES, ADDING IN OLD PARTIAL PRODUCT  
;12828 C31? ;1----- BRANCH ON CARRY FROM PREVIOUS ADD

=;END

U 1134. 0000,033C,0180,F800,0000,113C

;12829  
;12830  
;12831 =0\* ;0----- CHECK FOR CARRY INTO HIGH PRODUCT

U 1136. 0819,0314,0580,F800,0000,113C

;12832  
;12833  
;12834 =0\* ;0----- PROPAGATE THE CARRY

U 113C. 0521,373C,0040,F800,148D,5262

;12835  
;12836  
;12837 =0\* ;0----- NO CARRY  
;12838 MULD.05: ALU\_Q, Q\_ALU.LEFT, SHIFT <D,Q,PSL<N>> LEFT ONE  
;12839 D\_D.[LEFT], SI/DIVD TO FORM 64-BIT PRODUCT IN <D,Q>  
;12840 STATE\_STATE\_ANDNOT.SHF.VAL, ; CLR STATE<0> IF FRACT<.5 (POLYD ONLY)  
;12841 SC\_FE, STATE0?, J/MULD.06 ; SC=EXP, SEPARATE OUT MULD FROM EMOOD/POLYD

U 113E. 0819,0014,0580,F800,0000,113C

;12842  
;12843  
;12844 =;END ;1----- CARRY FROM ADD  
;12845 D\_D+K[.1], J/MULD.05 ; PROPAGATE IT AND CONTINUE

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA' OE, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : MULD

B 11

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:12846 ;EXIT FROM MULD FOR ALL USERS (MULD, EMODD, POLYD)
:12847
:12848 ==10 ;0----- THIS IS MULD
:12849 MULD.06: Q_Q.LEFT, D_D.LEFT, ; WE WANT <D,Q> NORMALIZED FOR
:12850 SI7D:VD, ; ROUNDING - THE FIRST SHIFT IS FREE.
:12851 FE_K[.18], J/MULD.07 ; SET UP FE FOR PACKD, GO TEST IF NORM
:12852
:12853 :1----- POLYD/EMODD
:12854 STATE0?, RETURN12 ; TEST NORMALIZATION IN CASE ITS POLYD
:12855 =:END
:12856
:12857
:12858 MULD.07: R[R15]_D, K[.80], D31? ; SAVE PROD<H>, CHECK IF NORMALIZED
:12859
:12860 =110 :----- BRANCH ON D31 (PRODUCT NORMALIZED)
:12861 :0----- D31 IS 0
:12862 D_D.LEFT, Q_Q.LEFT, ; DOUBLE SHIFT PROD LEFT
:12863 SI/DIVD,
:12864 SC SC-K[.1]., ; DECREMENT EXP TO COMPENSATE FOR SHIFT
:12865 J/MULD.07 ; TEST AGAIN (GUARANTEED TO SUCCEED 2ND TIME)
:12866
:12867 :1----- ROUND PROD FRAC <L>, SET C31 FOR ROUNDING
:12868 Q_Q+K[.80], CLK.LBCC, ; GO TO PACK RESULT
:12869 J7PACKD
:12870
:12871 =:END
:12872
:12873 FRACTION MULTIPLY ROUTINE FOR MULTIPLY DOUBLE - MULTIPLIES
:12874 AN UNSIGNED 32-BIT MULTIPLIER BY AN UNSIGNED 31-BIT MULTIPLICAND.
:12875 LOGIC IS V E R Y PARALLEL TO INTEGER MULTIPLY - SEE COMMENTS THERE.
:12876 =0
:12877 MULDMPY: :0----- ENTERED WITH 'Z?' TEST FOR M'CAND=0
:12878 ALU_0(A), D_D.RIGHT2, ; MULTIPLICAND NOT ZERO - SETUP FOR LOOP
:12879 LAB_R[R15], SI/ZERO, ; D GETS M'CAND
:12880 SC_K[.F], MUL?, J/MULPAP ; LATCH M'CAND TO LB
:12881
:12882 :1----- SETUP LOOPCOUNT & GOTO MULTIPLICATION ROUTINE
:12883 D_0, Q_0, ALU_0(A), ; M'CAND IS 0
:12884 LAB_R[R15], ; LATCH M'CAND TO LB ANYWAY
:12885 J/MULPAP ; LATCH RC[T6] AND EXIT
:12886 =:END
  
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ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : MULD

C 1:

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	:12887 ;MULTIPLY LOOP HERE - ENTER VIA 'MUL?, J/MULPAP'	
	:12888	
	:12889 =000	
U 12F0, 0200,003E,0300,F930,4000,0002	:12890 MULPAP: LC_RC[T6], !MULP.DONE, RETURN? ;RETURN TO RETURN ADDR .DR. 2	
	:12891	
	:12892 =100	
U 12F4, 0281,2C3C,0740,F800,0084,B2F0	:12893 QD_QD.RIGHT2, MUL.0XT, J/MULPAP ;+0, 0XT	
U 12F5, 028D,2C14,0740,F800,0084,B2F0	:12894 QD_(Q+LB)D.RIGHT2, MUL.CXT, J/MULPAP ;+1, 0XT	
U 12F6, 0291,2C00,07C0,F800,0084,B320	:12895 QD_(Q-LC)D.RIGHT2, MUL.1XT, J/MULPAM ;-2, 1XT	
U 12F7, 028D,2C00,07C0,F800,0084,B320	:12896 QD_(Q-LB)D.RIGHT2, MUL.1XT, J/MULPAM ;-1, 1XT	
	:12897	
	:12898	
	:12899 =000	
U 1320, 020D,2016,0340,F930,4000,0002	:12900 MULPAM: LC_RC[T6], ALU Q+LB, Q_ALU, ;RETURN TO RETURN ADDR .DR. 2	
	:12901 MULP.DONE, RETURN? ;AFTER CORRECTING PRODUCT	
	:12902	
	:12903 =100	
U 1324, 028D,2C14,0740,F800,0084,B2F0	:12904 QD_(Q+LB)D.RIGHT2, MUL.0XT, J/MULPAP ;+1, 0XT	
U 1325, 0291,2C14,0740,F800,0084,B2F0	:12905 QD_(Q+LC)D.RIGHT2, MUL.0XT, J/MULPAP ;+2, 0XT	
U 1326, 028D,2C00,07C0,F800,0084,B320	:12906 QD_(Q-LB)D.RIGHT2, MUL.1XT, J/MULPAM ;-1, 1XT	
U 1327, 0281,2C3C,07C0,F800,0084,B320	:12907 QD_QD.RIGHT2, MUL.1XT, J/MULPAM ;-0, 1XT	

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1W124.MCR 600,1204] MICR02 11.(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : EMODF

D 11

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:12908 .TOC   "      F & D floating point : EMODF"
:12909
:12910 :EMODF (54) MULR.RF, MULRX.RB, MULD.RF, INT.WL, FRACT.WF
:12911 :ENTER WITH Q = MULR.RF, D = MULRX.RB AT C.FORK.
:12912
:12913 3C8:
:12914 EMODF: -----
:12915 Q_D,
:12916 D_Q(FRAC),
:12917 SC_Q(EXP),
:12918 SS_ALU15,
:12919 CHR.FLT.OPR,J/FL.ABS.1023
:12920
:12921 1023: FL.ABS.1023: ;ASSIGN THIS ADD BECAUSE PCS CALLS IT
:12922
:12923 :0★1★-----
:12924 D_D.LEFT.SI/ZERO,
:12925 RC[1] Q.OXT[BYTE],
:12926 CALL,INTERRUPT.REQ?.J/SPEC ;MOVE TO LEAVE ROOM FOR M'IER EXT'ER
:12927 ;RC 1 GETS M'IFP: EXT'ER (BYTE)
:12928 1033: ;ASSIGN THIS ADDRESS BECAUSE OF CONSTRAINT ON PREVIOUS INSTRUCTION
:12929 :1★1★----- ;RETURN FROM 'SPEC'
:12930 D_D(FRAC),
:12931 FE_D(EXP),CLK.UBCC,
:12932 LC_RC[1],
:12933 SS_SS.XOR_ALU15&SD_ALU15,
:12934 CHR.FLT.OPR ;GET M'CAND FRAC
:12935 =:END ;M'CAND EXP
:12936 R[R15] D,
:12937 SC SC+FE,
:12938 EA[U?] ;LATCH UP MULTIPLIER EXTENDER
:12939 ;SS GETS RESULT SIGN
:12940 ;CHECK FOR -0
:12941 =1001 :1001----- ;R15 GETS M'CAND
:12942 SC_K[ZERO], ;SC GETS SUM OF EXP'S
:12943 RC[1] K[ZERO], ;M'IER OR M'CAND = 0?
:12944 D_0,q_0.SET.CC(INST),
:12945 J7EMODF.7 ;PROD = 0 (M'IER IS 0)
:12946
:12947 :1011----- ;PROD .NE. 0
:12948 RC[70] D.LEFT.SI/ZERO, ;RC 0 GETS M'CAND * 2
:12949 SC_SC-R[.80].J/EMODF.2 ;SAVE EXP WITH BIAS ADJUSTED
:12950
:12951 :1101----- ;PROD = 0 (M'IER, M'CAND ARE 0)
:12952 SC_K[ZERO],
:12953 RC[1] K[ZERO],
:12954 D_0,q_0.SET.CC(INST),
:12955 J7EMODF.7 ;PROD SET TO 0
:12956
:12957 :1111----- ;PROD SET TO 0
:12958 SC_K[ZERO],
:12959 RC[1] K[ZERO],
:12960 D_0,q_0.SET.CC(INST),
:12961 J7EMODF.7 ;PROD SET TO 0
:12962
  
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U 03C8, 0901,203C,01E1,F800,0888,7023

U 1023, 0503,AE3D,0180,F988,0000,037E

U 1033, 0901,003C,0185,F908,0918,739D

U 139D, 0001,123C,0180,FAF8,0080,9299

U 1299, 0F18,C038,19F8,F988,00F4,703E

U 1298, 0021,003C,4180,F980,0084,B3A4

U 129D, 0F18,C038,19F8,F988,00F4,703E

U 129F, 0F18,C038,19F8,F988,00F4,703E

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 E 11  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Sequence 340  
 : FLOAT .MIC [600,1204] F & D floating point : EMODF Page 339

U 13A4, 0811,2030,41FC,FA78,0104,B20C :12962 EMODF.2:  
 :12963 LAB\_R[R15], SD\_SS,  
 :12964 ALU\_Q.OR.LC, D\_ALU,  
 :12965 Q\_0, FE\_SC-K[.80] ; LATCH M'CAND  
 :12966 ; D GETS FULL 32 BIT MULTIPLIER  
 :12967 ; UNBIAS PRODUCT EXPONENT TO FE  
 :12968 ;  
 :12969 ; A NOTE ON THE MULTIPLICATION:  
 :12970 ; THE MULTIPLICAND HAS BIT 31=0, BIT 30=1  
 :12971 ; THE MULTIPLIER HAS BIT 31 = 1. ALL BITS ARE SIGNIFICANT  
 :12972 ; THE MULTIPLICATION IS CARRIED TO 66 BITS (17 ITERATIONS) SO THE LAST  
 :12973 ; ITERATION WILL THINK THE MULTIPLIER IS POSITIVE.  
 :12974 ; THEREFORE THE PRODUCT WILL BE SHIFTED 3 BITS RIGHT FROM WHAT IT  
 :12975 ; WOULD HAVE BEEN IF BOTH FRACTIONS HAD BEEN NORMALIZED AND THE  
 :12976 ; MULTIPLICATION CARRIED TO 64 BITS.  
 :12977 =0\* :0\*-----;  
 :12978 D\_D.RIGHT2,SI/ZERO, ; SHF'G FOR MULTIPLICATION  
 :12979 LTC\_RC[T0], ; LATCH M'CAND \* 2  
 :12980 SC\_K[.10], ALU\_O(A), ; SETUP LOOP COUNT AND ALU0-1 LATCHES  
 :12981 CALL,MUL?,J/MUL\_PP.4 ; CALL MUL SUBRT, GUARDING AGAINST SC=0  
 :12982 ;1\*-----;  
 :12983 RC[T1]\_0, NZ\_ALU.V&C\_0, ; RETURN  
 :12984 SC\_K[.3], ; SET UP RC[T1] AND CC'S FOR CVTFI  
 :12985 D\_Q,Q\_D ; SET UP TO SCALE PRODUCT  
 :12986 ; SWAP SO D GETS PROD<H>, Q PROD<L>  
 U 120C, 0203,0C3D,6580,F900,0084,6354 :12987 ;-----;  
 :12988 SC\_FE, D\_DAL.SC, Q\_0 ; SCALE PROD SO D HAS  
 :12989 ; 31/32 SIGNIFICANT BITS  
 :12990 ; \*\*\*\*\* ENTRY POINT FOR FPA \*\*\*\*\*  
 :12991 ; D HAS FRAC, SC HAS UNBIASED EXP, SS&SD HAVE RESULT SIGN, RC[T1]=0, Z=1  
 :12992 =0\*\*1\* :12993 EMODF.6:;0\*\*1\*-----;  
 :12994 SC\_SC-SHF.VAL,FE\_EALU, ; NORMALIZE  
 :12995 D\_DAL.NORM,  
 :12996 CALL, J/CVTFI.1 ;  
 :12997 ;  
 :12998 EMODF.7:  
 :12999 ;1\*\*1\*-----;  
 :13000 IDE[T0]\_P, Q\_0, D\_RC[T1], ; SET UP TO SHIFT FRACTION  
 :13001 SC? ; BUT DON'T SHIFT IF NUM<1.0  
 :13002 ;  
 U 103E, 0810,1438,C1F8,3D08,0000,1305 :13003 =101 ;101-----;  
 :13004 SC\_SC+K[.80], J/EMODF.8 ; BRANCH ON SC (NUM => 1.0)  
 :13005 ; NUM<1.0 - RF-BIAS EXPONENT  
 :13006 ;  
 U 1305, 0000,003C,4180,F800,0084,93A6 :13007 ;111-----;  
 :13008 SC\_K[.80], D\_DAL.SC ; NUM => 1.0 - THROW AWAY INTEGER  
 U 13A5, 0D00,003C,01F8,F800,0081,102E ;  
 U 102E, 0E00,003D,0180,F800,018C,A946 ;  
 U 1307, 0D00,003C,4180,F800,0084,73A6 ;

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204]  
; P1WT24.MCR 600,1204] MICRO2 1L(03) F & D floating point

F & D floating point 14-Jan-82  
14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124

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U 13A6, 0E00,0D3C,4180,F800,008C,B2D9

:13008 EMODF.8:  
:13009  
:13010 SC SC-SHF.VAL  
:13011 D\_BAL.NORM. K[.80].  
:13012 D\_NE.0?  
:13013 ==01  
:13014 EMODF.9:

:13015 :\*01----- D=0  
:13016 ID[T1] D, SC\_0(A), MAKE FRACTION A TRUE ZERO  
:13017 STATE 0(A), CLEAR STATE FOR DEST STORE FLAGS  
:13018 SGN/C[R].SD+SS,  
:13019 J/EMODFD GO STORE THE RESULTS  
:13020

U 12D9, 0003,003C,C587,3C00,1488,72A7

:13021 :\*11----- ROUND FRACTION  
:13022 D\_D+K[.80], CLK.UBCC  
:13023

U 13AC, 0000,033C,0180,F800,0100,D210

:13024 FE\_SC+1, C31? TEST FRACTION OVERFLOW FROM ROUND  
:13025

U 1210, 0808,0038,0180,F800,0000,13AD

:13026 :0\*----- NO OVERFLOW - USE UNINCREMENTED EXP  
:13027 EALU SC, D\_PACK.FP.  
:13028 J/EMODF.10

U 1212, 0808,0038,0180,F800,0081,73AD

:13029 :?\*----- OVERFLOW - USE INCREMENTED EXP  
:13030 GET LEFTOVER FRACTION PART  
:13031 EALU FE, SC\_FE,  
:13032 D\_PACK.FP, J/EMODF.10  
:13033

U 13AD, 0001,543C,1980,F800,5484,72A5

:13034 EMODF.10:  
:13035 .  
:13036 ALU D, N AMX.Z TST, SET COND CODES FROM FRACT  
:13037 WORD, INTPT\_STROBE.  
:13038 STATE K[ZERO],  
:13039 SC\_K[ZERO], SC?  
:13040 SET FOR FLOAT, TEST FOR UNDERFLOW  
:13041

U 12A5, 0F03,003D,0180,F800,0050,12AC

:13042 :0101----- FLOATING UNDERFLOW - MAKE FRACT=0  
:13043 ALU 0(A),N&Z\_ALU.V&C\_0,D\_0.  
:13044 CALL[PSLFU]

U 12A7, 0000,1A3C,31F0,2C00,0000,108C

:13045 EMODFD: :0111----- \*\* EMODD ENTERS HERE \*\*  
:13046 Q\_ID[CES],  
:13047 PSL.V?.J/EMODF.11 SEE IF WE HAD AN INTEGER OVERFLOW  
:13048

U 12AD, 0F03,003C,01F8,F988,0000,108C

:13049 :1101----- RETURN HERE IF PSL<fu>.eq.0(SC.eq.0)  
:13050 Q\_0,D\_0,RCE[T1]\_0.J/EMODF.11 CLEAR FRACT (INT=0 BY IMPLICATION)  
:13051

U 12AF, 0018,0038,F580,F988,0000,12B4

:13052 :13053 :1111----- RETURN HERE IF PSL<fu>.er 1(SC.ne.0)  
:13054 RCE[T7]\_K[A],J/FLOATFAULT T7 GETS UNDERFLOW TRAP CODE

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 ; FLOAT .MIC [600,1204] F & D floating point : EMODF

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U 108C, 0810,0E39,C580,3D08,0080,C47E :13055 108C: ;ASSIGN THIS ADDRESS BECAUSE PCS CALLS IT  
 :13056 EMODF.11:  
 :13057 :00\*1100-----; \*\* EDIV ENTERS HERE \*\*  
 :13058 SC SC+1.  
 :13059 ID[T1] D, D RC[T1],  
 :13060 CALL,INTERRUPT.REQ?.  
 :13061 J/ASPC : SAVE FRACT<H>, GET FRACT<L>  
 :13062 : EVALUATE INT.WL  
 U 108E, 0819,2030,65E0,F800,0000,13B4 :13063 108E: ;ASSIGN THIS ADDRESS BECAUSE OF CONSTRAINT ON PREVIOUS INSTRUCTION  
 :13064 :00\*1110-----; INTEGER OVERFLOW OCCURRED  
 :13065 Q,D,D Q.Q.OR.K[.10].  
 :13066 J7EMODF.V : SET INTEGER OVERFLOW CODE IN C.E.S.  
 :13067 :  
 U 10EC, 0C01,003C,0180,F990,5400,D084 :13068 10EC: ;ASSIGN THIS ADDRESS BECAUSE OF CONSTRAINT ON PREVIOUS INSTRUCTION  
 :13069 :11\*1100-----; RETURN 60: INT.WL IS MEM MODE  
 :13070 RC[T2]\_D,  
 :13071 D\_Q,  
 :13072 STATE STATE+1.  
 :13073 INTRPT.STROBE,  
 :13074 J/EMODF.12 : SAVE INT.WL ADDR  
 :13075 : D GETS FRACT <L>  
 :13076 : MARK FLAG FOR INT.WL R MODE  
 U 10ED, 0C40,0038,0180,F990,5C00,1084 :13077 10ED: ;ASSIGN THIS ADDRESS BECAUSE OF CONSTRAINT ON PREVIOUS INSTRUCTION  
 :13078 :11\*1101-----; RETURN 61: INT.WL IS R MODE  
 :13079 D\_Q,  
 :13080 RC[T2]\_RLOG.RIGHT,  
 :13081 INTRPT.STROBE,  
 :13082 J/EMODF.12 : SAVE REG # FOR INT.WL  
 :13083 = EMODF.V:-----  
 U 13B4, 0C00,003C,3180,3C00,0000,108C :13084 :ID[CES] D, D\_Q.  
 :13085 J/EMODF.11 : WRITE CES WITH TRAP CODE, GO STORE RESULTS

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 H 11  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Fiche 2 Frame H11 Sequence 343  
 : FLOAT .MIC [600,1204] F & D floating point : EMODF Page 342

U 1084, 0000,0E3D,C980,3C00,0080,C47E	:13086 =00*****0	
	:13087 EMODF.12:-----;	
	:13088 ID[T2] D, SC SC+1.	: T2 SAVES FRACT <L>, SC GETS 2/4 (FLT/DBL)
	:13089 CALL,INTERRUPT.REQ?,	
	:13090 J/ASPC	: EVALUATE FRACT.WX MODE
U 10E4, 0001,003C,0980,F9A0,1404,9114	:13091	
	:13092 =11*****0;-----;	: RETURN 60: FRACT.WX IS MEM MODE
	:13093 RC[T4] D,	: SAVE FRACT.WX ADDR
	:13094 STATE STATE+K[.2].	: MARK FOR MEM MODE FOR FRACT
	:13095 J/EMODF.14	: GOTO PROBE FRACT.WX
U 10E5, 0000,173C,C1F0,2C00,0000,12EA	:13096	
	:13097	
	:13098 Q_ID[T0],	: RETURN 61: FRACT.WX IS R MODE
	:13099 STATE0?,J/EMODF.16	: GET BACK INT.WL
	=;END	: INT.WL IS R OR M MODE?
U 1114, 0601,003D,01E0,F800,0200,0D0D	:13100	
	:13101	
	:13102	
	:13103 =0 EMODF.14:-----;	: SETUP FRACTION ADDR FOR PROBE SUBROUTINE
	:13104 VA D,Q,D,	: GET D SHIFTED FOR PAGE BOUNDARY TEST
	:13105 D,D,RIGHT,	: GOTO PROBE FRACT.WX BEFORE WRITING ANY
	:13106 CALL,J/PRB.W	
U 1115, 0010,1738,C1F0,2D20,0200,12EA	:13107	
	:13108 ;1-----;	: PROBE OK
	:13109 Q_ID[T0],	: GET BACK INT.WL
	:13110 VA RC[T4],	: GET BACK ADDR
	:13111 STATE0?,J/EMODF.16	: IS INT.WL MEM OR R MODE?
U 12EA, 0C10,0038,C5F0,2D10,0083,1385	:13112	
	:13113	
	:13114 =;END EMODF.16:-----;	: INT.WL IS R MODE
	:13115 D,Q,Q_ID[T1].	: D GETS INT, Q GETS FRACT.WX
	:13116 ST RC[T2](EXP),	: GET BACK REG #
	:13117 J/EMODF.17	
U 12EB, 0C10,0038,C5F0,2D10,0200,1386	:13118	
	:13119 ;1-----;	: INT.WL IS MEM MODE
	:13120 D,Q,Q_ID[T1].	: D GETS INT, Q GETS FRACT.WX
	:13121 VA RC[T2],	: GET ADDR
	:13122 J/EMODF.20	
U 13B5, 0C01,173C,0180,F8E8,0000,12F1	:13123	
	:13124	
	:13125 =;END EMODF.17:-----;	
	:13126 R(SC) D,D_Q.	: WRITE INT.WL
	:13127 STATE? :	: IS FRACT MEM OR R MODE?
U 12F1, 0001,163C,C9F0,2CD8,0000,1008	:13128	
	:13129	
	:13130 =01 EMODF.18:-----;	: R MODE
	:13131 R(PRN) D,	: WRITE FRACT.WF OR FRACT.WD <H>
	:13132 Q_ID[T2],	: GET BACK FRACT <L>
	:13133 STATE7-4?,J/EMODF.19	: EMODF OR EMODD?
U 12F3, 0010,D638,01C0,3108,0000,100C	:13134	
	:13135 ;1-----;	: MEM MODE
	:13136 CACHE D[INST.DEP].	: WRITE FRACT.WF OR FRACT.WD <H>
	:13137 Q_RC[T1],	: GET BACK FRACT <L>
	:13138 STATE7-4?,J/EMODF.22	: EMODF OR EMODD?
	:13139 =;END	

ZZ-ES0AA-124.0 : FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 I 11  
 P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Sequence 344  
 ; FLOAT .MIC [600,1204] F & D floating point : EMODF Page 343

U 1008, C000,003C,0180,F804,4000,0062	:13140 =1**0 ;0-----;	EMODF:
	:13141 EMODF.19:CLR.IB.OPC,PC_PC+1, J/IRD	UPDATE IB, PC
	:13142 ;-----;	GOTO NEXT INSTR
	:13143 ;-----;	
	:13144 ;1-----;	EMODD:
	:13145 R(PRN+1) Q,	WRITE FRACT.WD <L>
	:13146 CLR.IB.OPC,PC_PC+1, J/IRD	UPDATE IB, PC
	:13147 ;-----;	GOTO NEXT INSTR
	=;END	
	:13148 ;-----;	
	:13149 ;-----;	
U 1009, C001,203C,0180,F8E4,4000,0062	:13150 EMODF.20:-----;	
	:13151 CACHE_D[LONG]	STORE INT.WL
	:13152 ;-----;	
	:13153 ;-----;	
	:13154 VA RC[T4],D Q,	SET FRACT.WX ADDR
	:13155 STATE1?,J/EMODF.18	FRACT.WX MODE R OR MEM?
	:13156 ;-----;	
	:13157 =1**0	
U 100C, C000,003C,0180,F804,4000,0062	EMODF.22:;0-----;	EMODF
	:13158 CLR.IB.OPC,PC_PC+1, J/IRD	UPDATE IB, PC
	:13159 ;-----;	GOTO NEXT INSTR
	:13160 ;-----;	
	:13161 ;-----;	
	:13162 ;1-----;	EMODD
	:13163 D Q,	GET FRACT.WD <L>
	:13164 VA VA+4,	INC ADDR
	:13165 J/STOR.L	
U 100D, C000,003C,0180,F803,0000,03FD	=;END	
	:13166 ;-----;	

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 J 11 Fiche 2 Frame J11 Sequence 345  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 344  
 ; FLOAT .MIC [600,1204] F & D floating point : EMODD

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:13167 .TOC   "      F & D floating point : EMODD"
:13168
:13169 :EMODD (74) MULR.RD, MULRX.RB, MULD.RD, INT.WL, FRACT.WD
:13170 ;ENTER WITH <RC 0, Q> = MULR.RD, D = MULRX.RB AT C.FORK.
:13171
:13172 : COMPUTATIONAL METHOD - THE EXISTING CROSS-MULTIPLY TECHNIQUE,
:13173 WHICH WORKS FINE FOR MULD AND POLY, FALLS 1 BIT SHORT
:13174 IN ACCURACY FOR EMODD. TO GET AROUND THIS, SPECIAL CODE IN THE
:13175 MULTIPLY DOUBLE SUBROUTINE (TRIGGERED BY A STATE BIT) DELETES
:13176 THE NORMALIZE BIT OF THE EXTENDED ARGUMENT, REDUCING ITS ACCURACY
:13177 TO 63 BITS. AFTER THE MULTIPLY IS DONE, MORE SPECIAL CASE CODE
:13178 (IN EMODD THIS TIME) ADDS THE NON-EXTENDED ARGUMENT INTO THE
:13179 PRODUCT IN SUCH A WAY AS TO CONSTITUTE THE 64TH MULTIPLY STEP.
:13180 ; THIS SEEMS TO YIELD THE DESIRED ACCURACY.
:13181
:13182 386:
:13183 EMODD: -----
:13184     RC[T4]_D.OXT[BYTE],          ; GET 8 BIT EXT M'IER
:13185     D.Q,                      ; MOVE MULR <L> TO D
:13186     CALL,INTERRUPT.REQ?,J/SPEC ; EVALUATE MULD.RD
:13187
:13188 396: -----
:13189     [LC_RC[T2],J/FL.ABS.1043 ; RETURN WITH MULD IN <RC 2, D>
:13190
:13191 1043:                         ; ASSIGN THIS ADD BECAUSE PCS CALLS IT
:13192 FL.ABS.1043: -----
:13193
:13194     J/EMODD.1                  ; ** HACK TO AVOID CHANGING PROM **
:13195
:13196 =0**01: -----
:13197 EMODD.1: RC[T1] LC, STATE_K[.3],; UNPACK AND MULTIPLY THE FRACTIONS
:13198           CALLE[MULD.00]        ; MULD HAS SPECIAL-CASE EXTENDER CODE
:13199
:13200 =1**01: 0-----: PRODUCT = 0
:13201     ID[T0]_D, STATE_FE,       ; PREPARE TO SHARE CODE WITH EMODF
:13202     RC[T1]_0, N8Z_A[J.V&C_0,; ZERO INTEGER AND FRACTION PARTS
:13203           J/EMODD.6            ; AND GO STORE IT ( MULD LEAVES 10 IN FE! )
:13204
:13205     1-----: PRODUCT .NE. 0
:13206     RC[T2]_Q, STATE_K[.10],; SAVE LOW PRODUCT FRACTION, SET DBL FLAG
:13207           Q_0                 ; CLEAR Q FOR CONSTRAINT HACKERY
:13208 =:END
  
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ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 K 11  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Fiche 2 Frame K11 Sequence 346  
 : FLOAT .MIC [600,1204] F & D floating point : EMODD Page 345

U 1041, 0010,0D39,41C0,F910,0184,B2FA  
 U 1051, 0810,1A38,C1F8,3D10,1500,101C  
 U 101C, 0D10,1438,C9C0,3D08,0010,1025  
 U 101E, 0D10,1438,C9C0,3D08,1410,5025  
 U 1025, 0C10,1B39,41C0,F910,0184,867B  
 U 1027, 0C01,003C,C9F0,2D90,0000,138E  
 U 1035, 0098,1638,01C0,F800,1504,7208  
 U 1208, 0001,203C,0180,F800,14A2,92A7  
 U 1209, 0001,203C,0180,F800,1482,92A7  
 U 13BE, 0D03,003C,0180,F800,0088,73C0  
 U 13C0, 0001,003C,01E0,F800,0010,1025

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:13209 :      ** FPA FMODD ENTERS HERE WITH MANTISSA IN <D,RC[T2]>, EXP IN SC,
:13210 :      STATE=10, SIGN IN SS, Q=0.
:13211 :
:13212 =0**** :-----  

:13213 EMODD.2: Q RC[T2], SC_SC-K[.80], FE_EALU, : GO NORMALIZE FRACT AND GET INTEGER PART  

:13214          D31?, CALL[EMODD.5] : SAVE EXPONENT IN FE
:13215
:13216
:13217 -----  

:13218 ID[T0]_D, D RC[T2], Q_0, FE_STATE, PSL.V? : RETURN FROM CVTFI - STORE INT FROM D.  

:13219          Q_0, FE_STATE, PSL.V? : GET MANTISSA<L> IN D, TEST INT OVFLO
:13220
:13221 =110* :0-----  

:13222          Q_RC[T1], CLK.UBCC, : NO OVERFLOW - LEAVE STATE=10  

:13223          ID[T2]_D, D DAL.SC, : GET MANTISSA<H> IN Q & SET Z ON IT  

:13224          SC?. J/EMODD.3 : DO 1ST PART OF 64-BIT FRACT SHIFT  

:13225          SC? : WHILE WE CHECK IF ITS NECESSARY
:13226          1-----  

:13227 STATE STATE_ANONOT.FE, : OVERFLOW
:13228          Q_RC[T1], CLK.UBCC, : CLEAR STATE TO INDICATE OVFLO
:13229          ID[T2]_D, D DAL.SC, : IF NUM=>1.0 WE WANT TO SHIFT THE INTEGER
:13230          SC? : PART OUT OF THE MANTISSA - START IT,  

:13231          SC? : AND TEST IF WE REALLY OUGHTA DO IT.
:13232 =0*101 :BRANCH ON SC.GT.0 (NUM=>1.0) - ALSO CALLSITE FOR ADDD/PACKD
:13233          0-----  

:13234 EMODD.3: D Q, Q RC[T2], ST_SC+RE[.80], FE_EALU, : NUM < 1.0 (ALSO NUM=>1.0 CASE JOINS IN HERE)
:13235          ALU?, CALL[ADDD.31] : GET UNSHIFTED FRACTION IN <D,Q>
:13236          J/EMODD.4 : PUT BIAS BACK INTO EXPONENT
:13237          1-----  

:13238          RC[T2]_D, D Q, Q_ID[T2], : USE ADDD TO NORMALIZE, ROUND & PACK
:13239          J/EMODD.4 : NUM => 1.0
:13240          1-----  

:13241          STATE_K[.8], FE_K[.8], Q_K[.8].RIGHT2, : SAVE NEW FRACT<L>, SET UP TO SHIFT
:13242          STATE4? : FRACT<H> LEFT TO DESTROY INT PART
:13243          SC_Q, J/EMODFD : ADDD.31/PACKD RETURNS HERE - RESULT IN <D,RC1>
:13244          SC_Q, J/EMODFD : MONKEY BUSINESS TO SET STATE=10, SC=2
:13245          SC_Q, J/EMODFD : SO WE CAN SHARE RESULT-STORE CODE WITH EMODF
:13246          SC_Q, J/EMODFD : MEANWHILE, TEST THE SAVED INT OVFLO FLAG
:13247 =:END
:13248 =***0 :0-----  

:13249          SET_V, STATE_STATE+FE, : INTEGER OVERFLOW OCCURRED
:13250          SC_Q, J/EMODFD : SET STATE=10, SET V BIT (PACKD CLEARS IT)
:13251          SC_Q, J/EMODFD : SET SC=2, SAVE PACKED RESULT<H>, JOIN EMODF
:13252          SC_Q, STATE_STATE+FE, : NO INTEGER OVERFLOW OCCURRED
:13253          J/EMODFD : SET SC=2, STATE=10 FOR EMODF
:13254          J/EMODFD : GO STORE THE RESULTS
:13255 =:END
:13256
:13257 EMODD.4: D_DAL.SC, SC_0(A) : MANTISSA SHIFT CONTINUED - SHIFT FRACT<H>
:13258
:13259
:13260          Q_D, ALU_D, CLK.UBCC, : SET Z ON HIGH LONGWD OF NEW FRACT
:13261          J/EMODD.3 : AND GO NORMALIZE, ROUND AND PACK IT
  
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ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 L 11  
: P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124  
: FLOAT .MIC [600,1204] F & D floating point : EMODD Fiche 2 Frame L11 Sequence 347  
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:13262 : INTERFACE BETWEEN EMODD AND CVTFI - CALLED AS MICROSUBROUTINE  
:13263 :  
:13264 :  
:13265 ==10 :-----: BRANCH ON D31 (PRODUCT IS NORMALIZED) (Q = 0)  
:13266 :0-----: PRODUCT NOT NORMALIZED  
:13267 EMODD.5: ALU 0+KE[1], Q Q.LEFT, : SHIFT THE FRACTION LEFT A BIT  
:13268 D D.LEFT, SI/DIVD,  
:13269 SC\_SC-K[1], FE\_EALU : ADJUST EXPONENT TO MATCH  
:13270 :  
:13271 :1-----: PRODUCT NORMALIZED  
:13272 RC[T1]\_0, J/CVTFI.1 : INITIALIZE MANTISSA<H> HOLDER & CALL CONVERT  
:13273 =;END :  
:13274 :  
:13275 :  
:13276 :  
:13277 :-----: CONTINUATION OF EMODD PROD=0 CASE  
:13278 EMODD.6: SGN/CLR\_SD+SS, : CLEAR SIGNS (MAY NOT BE NECESSARY)  
:13279 SC\_K[2], J/EMODF.11 : SET D.P. FLAG IN SC AND JOIN EMODF

M 11

Fiche 2 Frame M11      Sequence 348  
VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124      Page 347

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204]      F & D floating point 14-Jan-82  
P1W124.MCR 600,1204]      MICRO2 1L(03)      14-Jan-82 15:30:16  
; FLOAT .MIC [600,1204]      F & D floating point : POLYF

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:13280 .TOC   "      F & D floating point : POLYF"
:13281
:13282 :      POLYF (55) ARG.RF, DEGREE.RW, TBLADDR.AB
:13283 :ENTER AT C.FORK WITH Q HAS ARG.RX, D HAS DEGREE.RW.
:13284 :WHEN DONE, R0 = RESULT, R2 = 0, R1 = 0, R3 = TABLE ADDR + DEG*4 + 4.
:13285 :IN PROCESSING, R0 = PARTIAL RESULT, R2 = DEG, R1 = ARG, R3 = NEXT TABLE ADDR.
:13286
:13287 3C2:
:13288 POLYF: -----
:13289     D_D.OXT[WORD],J/POLYF.0           ; GET DEGREE.RW
:13290 0C2:
:13291 POLYF.FPD: -----
:13292
:13293     D_R[R2],Q_0,SC_K[.FFF8],          ; SETUP TO GET PC DELTA
:13294     J7FL.ABS.T01D                   ;
:13295
:13296 101D:                               ;ASSIGN THIS ADD BECAUSE PCS CALLS IT
:13297 FL.ABS.101D: -----
:13298     D_DAL.SC                      ; PC DELTA IN D[07:00]
:13299
:13300 =C0 :00-----;
:13301     PC&VA_D.OXT[BYTE]+PC,          ; BYPASS SPECIFIERS
:13302     CALL, J/SETFPD               ; NEED TO RE-SETUP ID[FPDA]
:13303
:13304 =10 :10-----;
:13305     Q_PC, J/BAKUP.PC            ; READ ERRORS COME HERE
:13306     BACKUP PC AND CAUSE A TRAP
:13307
:13308 :11-----;
:13309     INTRPT.STROBE, J/POLYF.2;    RETURN FROM SETFPD HERE
:13310     WASTE - HOWEVER TOO TOUGH TO SHARE SETFPD CALL
:13311
:13312 12C2:
:13313 POLY.C: -----; SET COND CODES AFTER DONE FOR BOTH POLYF/D
:13314     EALU SC,ALU_R[R0].          ; SC SHOULD HAVE THE EXP ID
:13315     SET.CC(INST)              ; SET COND CODES
:13316
:13317 POLY.0: -----; FLUSH IB
:13318     ALU PC,FLUSH.IB,          ; FLUSH IB IN CASE RE-ENTERED
:13319     J/IB.FILL
:13320
:13321 12C3: -----; SET COND CODES AFTER DONE FOR BOTH POLYF/D
:13322     EALU SC,ALU_R[R0].          ; SC SHOULD HAVE THE EXP ID
:13323     SET.CC(INST)              ; SET COND CODES
:13324     J/POLY.0                  ; GOTO FLUSH IB
:13325
:13326 448:
:13327 POLY.CC: -----
:13328     EALU SC,ALU_R[R0].          ; SET CC AFTER DONE FOR BOTH POLYF/D
:13329     SET.CC(INST)              ; SC SHOULD HAVE THE EXP ID
:13330     CLR.IB.OPC,PC_PC+1,J/IRD  ; SET COND CODES
:13331                           ; UPDATE IB, PC

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U 03C2, 0803,403C,0180,F800,0000,1012

U 00C2, 0800,003C,71F8,FA10,0084,701D

U 101D, 0D00,003C,0180,F800,0000,1310

U 1310, 0017,8015,0180,F801,0200,0E16

U 1312, 0014,0038,01C0,F800,0000,0EB8

U 1313, 0000,003C,0180,F800,4000,1082

U 12C2, 0000,C03C,0180,FA00,0070,13C3

U 13C3, 2014,0038,0180,F800,4200,00AB

U 12C5, 0000,C03C,0180,FA00,0070,13C3

U 0448, C000,C03C,0180,FA04,4070,0062

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA GE, WCS124  
 ; FLOAT .MIC [600,1204] F & D floating point : POLYF

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Fiche 2 Frame N11

Sequence 349  
 Seguence 349

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U 1012, 0C19,0v24,8DE0,F800,0010,13C4

:13332 1012: ;ASSIGN THIS ADDRESS BECAUSE PCS CALLS IT  
 :13333 POLYF.0:  
 :13334 ALU.D.ANDNOT.K[.1F], : CHECK IF DEGREE > 31  
 :13335 CLK.UBCC, : CLOCK IN ALU.Z  
 :13336 D\_Q,Q\_D : D GETS ARG, Q GETS DEGREE  
 :13337 =;END  
 :13338 :  
 :13339 ID[T0] D, : TO SAVES ARG  
 :13340 ALU.Q(B), RC[T2] ALU, : RC 2 SAVES DEGREE, SET ALU.Z ON DEGREE  
 :13341 FE.D(EXP),CLK.UBCC, : FE GETS ARG EXP, CLOCK IN FOR ZERO CHECK  
 :13342 INTRPT.STROBE, : ENABLE INTERRUPTS  
 :13343 Z? : CHECK RANGE OF DEGREE IF LEGAL?

U 13C4, 001D,0138,C180,3D90,4118,70A2

:13344 =01\*\*\*\*0:-----  
 :13345 J/RSVOPR : NO: OUT OF RANGE  
 :13346 DEGREE > 31: ILLEGAL

U 10A3, 0001,0E3D,0180,F800,0800,047E

:13347 =01\*\*\*\*1:-----  
 :13348 ALU.D.CHK.FLT.OPR, : YES: IN RANGE  
 :13349 CALL,INTERRUPT.REQ?, : CHECK IF ARG IS -0  
 :13350 J/ASPC : GET COEF

U 10E3, 0058,0038,45E0,42F8,0000,13C5

:13351 =11\*\*\*\*1:-----  
 :13352 Q.D, : ASPC ALWAYS RETURNS 60 IN THIS CASE  
 :13353 D[LONG] CACHE, : TABLE ADDR  
 :13354 R[R15].ALU.RIGHT, : GET COEF CO  
 :13355 S1/ZERO,ALU\_K[.8000] : SETUP FOR 4080 (FP 1.)  
 :13356 =;END

U 13C5, 0001,003C,0180,F800,0800,13C9

:13357 ALU.D.CHK.FLT.OPR : CHECK 1ST COEF CO FOR -0

U 13C9, 0001,203C,C1F0,2E98,0000,1224

:13358 R[R3].Q,Q\_ID[T0] : R3 STORES TABLE ADDR, Q GETS ARG

U 1224, 0001,203D,C580,3F90,0000,13E8

:13359 =0 :  
 :13360 ID[T1].D, : T1 SAVES CO  
 :13361 ALU.Q, : R1 GETS ARG  
 :13362 LC.RC[T2]&R1.ALU, : LATCH DEGREE  
 :13363 CALL,J/POLY.PC : GO GET PC DELTA

U 1225, 0011,0030,C5F0,2E90,0000,1328

:13364 R[R2].D.OR.LC, : R2 GETS PC DELTA, DEGREE  
 :13365 Q\_ID[T1] : Q GETS CO

U 1328, 0811,2039,0180,F800,0088,6E16

:13366 =;END  
 :13367 =00 :  
 :13368 SC.Q(EXP), : SC GETS CO EXP  
 :13369 D[LC, : D GETS DEGREE  
 :13370 CALL,J/SETFPD : SET FPD

U 132A, 0014,0038,01C0,F800,0000,0EB8

:13371 =10 :  
 :13372 Q\_PC, J/BAKUP.PC : READ ERROR, POLYF FPD PACKING ROUTINE  
 :13373 BACK UP PC AND CAUSE EXCEPTION

U 1323, 0018,0038,41C0,FA78,0000,13CA

:13374 =;END  
 :13375 =11 :  
 :13376 Q\_K[.80],LAB\_R[R15] : GET 4080 (FP 1.)

U 13CA, 001C,0014,C5F0,2E80,0000,13CB	:13387	-----	
	:13388	Q_ID[.1],	GET BACK 1ST COEF C0
	:13389	R[R0]_LA+Q	RUNNING SUM IS 1.0 BEFORE C0 TESTED FOR -0
	:13390	-----	
	:13391	-----	
U 13CB, 0000,003C,0180,FA18,0000,13CD	:13392	LAB_R[R3]	LATCH TABLE ADDR
	:13393	-----	
	:13394	-----	
	:13395	R[R3]&VA_LA+K[.4].	INC TABLE ADDR
	:13396	SGN/CLR_SD+SS.	EASE UP ON EALUZ CONSTRAINT
U 13CD, 0018,0D14,1187,FA98,0200,1064	:13397	D.NE.0?	IS DEGREE 0?
	:13398	-----	
	:13399	=10* :0-----	DEGREE = 0
	:13400	CLR.FPD,	CLR PSL <FPD> BIT
U 1064, 0001,343C,0180,FA80,2000,1301	:13401	R[R0]_Q,	R0 GET COEF C0
	:13402	SC.GT.0?,J/POLYF.5	IS C0 0?
	:13403	-----	
	:13404	-----	
U 1066, 0001,323C,0180,FA80,4000,1082	:13405	R[R0]_Q, INTRPT.STROBE,	DEGREE .NE. 0
	:13406	EALU.Z?	R0 GETS COEF C0
	:13407	=:END	IS ARGUMENT 0?
	:13408	-----	
	:13409	=*01*-----	
	:13410	POLYF.2:0-----	NO:
	:13411	Q_R[R1](FRAC).	ARG FRAC
	:13412	SC_R[R1](EXP).	ARG EXP
U 1082, 0000,0E3C,01C9,FA08,0083,1336	:13413	SS_ALU15,	ARG SIGN
	:13414	INTERRUPT.REQ?,	
	:13415	J/POLYF.8	
	:13416	-----	
	:13417	-----	
U 1086, 0118,0038,1980,FA80,0000,13D0	:13418	R[R0]_K[ZERO],	YES: ARGUMENT = 0
	:13419	D_D.LEFT2	ZERO OUT THE PARTIAL PRODUCT
	:13420	=:END	D GETS DEGREE*4
	:13421	-----	
U 13D0, 001C,2014,0180,FA98,0000,13D1	:13422	R[R3]_LA+D	ADVANCE THE EXECUTION OF THE POLYNOMIAL
	:13423	-----	TO THE LAST COEFFICIENT
	:13424	-----	
U 13D1, 0018,8038,0580,FA90,0000,1082	:13425	R[R2]_K[.1], DT/BYTE,	BY BUMPING THE TABLE ADDR AND DEGREE
	:13426	J/POLYF.2	NOW JOIN THE ORDINARY ITERATION CODE
	:13427	-----	
	:13428	=*01-----	
U 1301, 0018,0038,1980,FA80,0000,1303	:13429	POLYF.5:0-----	C0 IS 0
	:13430	R[R0]_K[ZERO]	SET RESULT 0
	:13431	-----	
	:13432	-----	
U 1303, 0003,003C,0180,FA90,0000,13E6	:13433	R[R2]_C, J/POLYF.22	C0 IS NOT 0
	:13434	=:END	CLR R2 AND GO EXIT

	:13435 =110	
	:13436 POLYF.8:;0-----	NO INTERRUPT REQ
	:13437 D_R[R0](FRAC),	GET PARTIAL RESULT FRAC
	:13438 FE_R[R0](EXP),	PARTIAL RESULT EXP
	:13439 SS_SS.XOR.ALU15&SD_ALU15,;	SS PARTIAL RESULT SIGN
	:13440 CLR.UBCC,	CLOCK IN IF ZERO (EALU.Z)
	:13441 J/POLYF.9	
	:13442	
	:13443 ;1-----	YES: INTERRUPT REQ
	:13444 J/POLY.INT	INTERRUPT ENTRY TO CLR TP AND BACKUP PC,R'S
	:13445 =;END POLYF.9:-----	
	:13446 FE_SC+FE_SD_SS,	ADD EXP'S, SD GETS PART PROD SIGN
	:13447 RC[T0] Q,Q_0,	
	:13448 EALU.Z?	PARTIAL RESULT = 0?
	:13449	
	=*011 :0-----	NO:
	:13450 LC_RC[T0],	LATCH M'CAND * 2 (ARG)
	:13451 SC_K[.FFF9],	SETUP DAL SHF COUNT
	:13452	
	:13453 J/POLYF.10	
	:13454	
	:13455	
	:13456 ;1-----	YES:RETURN NEXT COEF AS PARTIAL PROD
	:13457 SC_K[.7F],D_0,	PARTIAL RESULT EXP SET TO 0
	:13458 SGN/CLR_SD+SS,	FRAC SET TO 0, SIGN SET TO 0
	:13459 VA_R[R3]	LATCH TABLE ADDR
	:13460 =;END	
	:13461 ;	
	:13462 ;NOTE THAT THE NORMAL ADD ROUTINE IS SKIPPED IF THE PARTIAL PRODUCT	
	:13463 ;IS ZERO BECAUSE THE ADD ROUTINE DOESN'T ALWAYS HANDLE THE ZERO CASE	
	:13464 ;CORRECTLY	
	:13465 ;	
	:13466 -----	
	:13467 D[LONG]_CACHE	GET NEXT COEFFICIENT
	:13468	
	:13469	
	:13470 R[R0] D,D_D(FRAC),	SAVE COEF,UNPACK IT AND TEST FOR RES OPR
	:13471 SC_D(EXP),SS_ALU15,	
	:13472 CLR.UBCC,CHK.FLT.O'R	
	:13473	
	:13474 -----	
	:13475 R[R3]&VA_LA+K[.4].	INCREMENT TABLE ADDRESS
	:13476 SC_NE.0?	IS COEF ZERO?
	:13477	
	=1011 :1011-----	SC=0
	:13478 R[R0]_K[ZERO]	MAKE SURE ZERO IS CLEAN
	:13479	
	:13480	
	:13481 :1111-----	SC_NE ZERO
	:13482 LAB_R[R2],FE_K[.1F],	LATCH DEGREE,SET UP FE
	:13483 J/POLYF.17	REJOIN CODE AFTER ADD
	:13484	

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204]  
; P1W124.MCR 600,1204]  
; FLOAT .MIC [600,1204]

F & D floating point  
MICR02 1L(03) 14-Jan-82 14-Jan-82 15:30:16

F & D floating point : POLYF

D 12

14-Jan-82

VAX11/780 Microcode : PCS 0 , FPLA 0E, WCS124

Fiche 2 Frame D12

Sequence 352

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U 13DC, 0D50,0038,8580,FAF8,0084,7214

U 1214, 0203,0C3D,0180,FA78,0000,0350

U 1216, 0C00,003C,0DE0,F800,0084,73DD

U 13DD, 0D00,003C,01F8,F800,0081,13E0

U 13E0, 0E00,003C,0180,FA18,028C,B3E1

:13484  
:13485 POLYF.10:  
:13486 D\_DAL.SC,  
:13487 R[R15].LC.RIGHT,SI/ZERO,  
:13488 SC\_K[.T]  
:13489  
:13490 =0\* :0-----  
:13491 D\_D.RIGHT2,SI/ZERO,  
:13492 ALU\_0(A)  
:13493 LAB\_R[R15]  
:13494 CALC,MUL?,J/MULPP  
:13495  
:13496 :1-----  
:13497 SC\_K[.3],  
:13498 D\_Q,Q\_D  
:13499 =;END  
:13500 SC\_FE, D\_DAL.SC, Q\_0  
:13501  
:13502  
:13503  
:13504 SC\_SC-SHF.VAL,  
:13505 D\_BAL.NORM,  
:13506 VA\_R[R3]  
: SHF M'IER IN POSITION  
: R15 GET M'CAND (ARG)  
: LOOP CT SET FOR 13. LOOPS  
: BEGIN SHF'G M'CAND  
: LATCH ALU[01:00]  
: LATCH M'CAND  
: CALL MUL SUBRTN - PROD HAS 4-5 LEADING 0'S  
: RETURN FROM MUL SUBRT  
: GET READY TO ALIGN RESULT FRACTION  
: D GETS HIGH PROD, Q GETS LOW PROD  
: FRACTION NOW HAS 31 OR 30 SIGNIFICANT BITS  
: NORMALIZE  
: LATCH DEGREE COUNT

	:13507	POLYF.12:	
	:13508		
	:13509	R[C[76]] ALU, ALU PACK.FP,	: SAVE PART PROD SIGN
	:13510	FE SC-R[.7F], C[K.UBCC,	: ADJUST RESULT EXP
	:13511	Q D	: Q GETS MUL RESULT
	:13512	D[LONG]_CACHE	: GET NEXT COEF
	:13513		
	:13514		
	:13515	Q Q.RIGHT, SI/ZERO,	: PUT PRODUCT FRACTION IN ADDD FORMAT
	:13516	R[R15] D, D D(FRAC),	: COEF FRAC
	:13517	SC_D(EXP), SS_ALU15, CHK.FLT.OPR	: COEF EXP, COEF SIGN, CHECK FOR -0
	:13518		
	:13519	=0*1**0110	
	:13520	:0*1**0110-----	
	:13521	D Q Q D,	: D GETS DST FRAC, Q SRC FRAC
	:13522	R[R3]&VA_LA+K[.4],	: UPDATE TABLE ADDR
	:13523	SC SC-FE, CLK.UBCC,	: GET EXP DIFF, CLOCK IN FOR EXP'S DIFF
	:13524	SC.GT.0?, CALL[POLYF.14]	: IS COEFF 0?
	:13525		
	:13526	=1*1**0110	
	:13527	:1*1**0110-----	: RESULT 0
	:13528	LAB_R[R2], J/POLYF.19	: LATCH DEGREE
	:13529		
	:13530		
	:13531	POLYF.13:	
	:13532	:1*1**1110-----	: RESULT NON-0, NO CARRY FROM FRAC
	:13533	LAB_R[R2],	: LATCH DEGREE
	:13534	FE R[.1F],	: SETUP TO DISREGARD UNDERFLOW FLAG
	:13535	SC?, J/POLYF.26	: CHECK FOR OVER/UNDER FLOW, 0, ETC.
	:13536		
	:13537	:1*1**111-----	: RESULT NON-0, CARRY FROM FRAC
	:13538	D D.RIGHT, SC SC+1	: ROUND UP BY 1
	:13539	SI/ZERO, J/POLYF.13	
	:13540		
	:13541	=*01	
	:13542	POLYF.14:	
	:13543	:*01-----	: COEFFICIENT IS 0
	:13544	SC FE, ALU_D, CLK.UBCC,	: SUM = PARTIAL PRODUCT, ROUNDED.
	:13545	J/NEGCK	: USE ADDF CODE TO CHECK FOR 0 AND ROUND
	:13546		
	:13547	:*11-----	: COEFFICIENT .NE. 0
	:13548	I[D[T1]] D, ALU RC[T6],	: SAVE DST OPR (PART PROD),
	:13549	SS_SS_XOR_ALU15&SD_ALU15,	: FIX SIGN INDICATORS FOR FADD
	:13550	SC.GT.0?	: SEE IF WE SHOULD NEGATE EXPONENT DIFF
	:13551	=101	
	:13552	:101-----	: EXP DIFF <= 0 - NO NEED TO NEGATE
	:13553	EALU?, J/ADDFSH	: BREAK OUT FADD CASES AND ADD
	:13554		
	:13555	:111-----	: EXP DIFF > 0 - MUST NEGATE
	:13556	ALU 0-K[SC], SC_ALU,	: NEGATE SC THRU MAIN DATA PATH
	:13557	EALU?, J/ADDFSH	: NOW GO DO THE FADD.
	:13558		
	:13559	YOU MAY ASK, WHY GO THROUGH THIS RIGAMAROLE WHEN WE HAVE AN EALU FUNCTION TO	
	:13560	TAKE THE NEGATIVE ABSVAL OF (SC-FE)? THE ANSWER IS THAT SINCE THE MULTIPLY IS	
	:13561	ALLOWED TO UNDERFLOW, THE RANGE OF THE EXPONENT DIFFERENCE IS LARGER THAN THE	
		SIZE OF THE NABS ROM.	

ZZ-ES0AA-124.0 : FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 F 12  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Sequence 354  
 ; FLOAT .MIC [600,1204] F & D floating point : POLYF Page 353

U 12D1, 0000,003D,3DF0,2C00,0000,12AE	:13562 ; COME HERE AFTER ADD WITH FRAC IN D, EXP IN SC, BEN/SC
	:13563 ;=0001
	:13564 POLYF.26:
	:13565 :0001-----; SC.eq.0, UNDERFLOW
	:13566 Q_ID[PSL],CALL[PSLFU.A] ; Get PSL<fu> & go see if it is set
	:13567
	:13568 :0011-----; SC.eq.[01 to FF], NO OVER/UNDERFLOW
	:13569 EALU SC,R[0] PACK.FP, ; R0 STORES RESULT
	:13570 FE_EALU,J/POLYF.17 ; FE GETS RESULT EXP TO SET CC LATER
	:13571
	:13572 :0101-----; SC.lss.0, UNDERFLOW
	:13573 Q_ID[PSL],CALL[PSLFU.A] ; Get PSL<fu> & go see if it is set
	:13574
	:13575 :0111-----; SC.gt.0, OVERFLOW
	:13576 D_K[.8], ; D GETS OVERFLOW TRAP CODE
	:13577 LAB_R[R3],J/POLYFFAULT ; FETCH TABLE ADDRESS
	:13578 =1101
	POLYF.19:
	:13579 :1101-----; RETURN HERE IF PSL<fu>.eq.0(SC.eq.0)
	:13580 R[0],FE_K[ZERO],J/POLYF.17 ; PRETEND UNDERFLOW DIDN'T HAPPEN
	:13581
	:13582
	:13583 :1111-----; RETURN HERE IF PSL<fu>.eq.1(SC.ne.0)
	:13584 D_K[A], ; D GETS UNDERFLOW TRAP CODE
	:13585 LAB_R[R3],J/POLYFFAULT ; FETCH TABLE ADDRESS
	:13586
	:13587
	:13588
	:13589 R[R2] LA-K[.1],BYTE. ; DECREMENT DEGREE COUNT IN R2<7:0>
	:13590 CLK.UBCC ; AND SET Z IF WE ARE DONE
	:13591
	:13592
	:13593 INTRPT.STROBE.Z? ; ENABLE INTERRUPTS - IS COUNT UP?
	:13594
	=0
	:13595 :0-----; NO:
	:13596 Q_R[R1](FRAC), ; ARG FRAC
	:13597 S_C_R[R1](EXP), ; ARG EXP
	:13598 SS_ALU15, ; ARG SIGN
	:13599 INTERRUPT.REQ?, ; ANY INTERRUPT REQUEST?
	:13600 J/POLYF.8 ; GOTO NEXT LOOP
	:13601
	:13602
	:13603 :1-----; YES: THIS IS THE END
	:13604 CLR.FPD,R[R2]_K[ZERO] ; CLEAR PSL<FPD>, CLEAR R2
	:13605
	:13606
	:13607 R[R1] K[ZERO],
	:13608 SUB/SPEC,J/POLY. C ; CLR R1
	GOTO SET COND CODES
U 13E3, 0018,8000,0580,FA90,0010,13E4	
U 13E4, 0000,013C,0180,F800,4000,1234	
U 1234, 0000,0E3C,01C9,FA08,0083,1336	
U 1235, 0018,0038,1980,FA90,2000,13E6	
U 13E6, 0018,003B,1980,FA88,0000,12C2	

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:13609 ; ROUTINE TO GET PC DELTA FOR POLY
:13610 POLY.PC:
:13611 -----: Q GETS PC
:13612 Q_0+PC.RLOG : PUSH RLOG SO PCSV REF WON'T KILL IT
:13613
:13614 -----: GET PC DELTA
:13615 D_Q-PCSV
:13616
:13617 -----: OEXT PC DELTA, SETUP TO SHIFT PC DELTA
:13618 D_D.OXT[BYTE],SC_K[.8],Q_0
:13619
:13620 -----: SHIFT PC DELTA, GET DEGREE FOR POLYD
:13621 D.DAL.SC,Q_ID[T0],RETURN1
:13622
:13623
:13624 =0*
:13625 POLY.INT:
:13626 :0*-----: PUT PC WHERE BAKUP.PC WANTS IT AND
:13627 Q_PC,CALL[BAKUP.PC] : GO DO IT
:13628
:13629 :1*-----: GO ALLOW INTERRUPT
:13630 J/INT.I
:13631
:13632
:13633 POLYFFAULT:
:13634 -----: Enter here with fault code in D
:13635 R[R3]_LA-K[.4],J/POLY.FAULT : DE-INCREMENT TABLE ADDRESS
:13636
:13637 POLYDFAULT:
:13638 -----: Enter here with fault code in D
:13639 R[R3]_LA-K[.8],J/POLY.FAULT : DE-INCREMENT TABLE ADDRESS
:13640
:13641 POLYFAULT:
:13642 -----: PUT FAULT CODE WHERE I WILL BE SAFE
:13643 R[CT7]_D
:13644
:13645 -----: TO VECTOR ID OF FLOATING FAULTS
:13646 R[CT0]_K[.34],STATE_0(A) : CLEAR STATE(WILL BE SET TO 1 LATER)
:13647
:13648 =00 :00-----: SET UP PC WHERE 'BAKUP.PC' WANTS IT
:13649 Q_PC,RC[PC.SV]_PC,CALL[BAKUP.PC] : GO BACK UP PC
:13650
:13651 =10 :10-----: RETURN HERE FROM 'BAKUP.PC'
:13652 Q_ID[PSL],STATE STATE+1,CALL[EXCPT1] : GET PSL INTO Q
:13653 :11-----: STATE=1 TO INDICATE PARAMETERS
:13654 :10-----: GO INITIALIZE FAULT
:13655
:13656
:13657
:13658 :11-----: RETURN HERE FROM 'EXCPT1'
:13659 D_RC[T7] : GET FAULT CODE
:13660
:13661 POLYFLOATFAULT.A:
:13662
:13663 R[SP]&VA_LA-K[.4],J/EXCPT2 : DEC STACK POINTER & GO PSH FLT CODE
  
```

ZZ-ESOAA-124.0 : FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 H 12  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 Fiche 2 Frame H12 Sequence 356  
 ; FLOAT .MIC [600,1204] F & D floating point : POLYD VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 355

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;13664 .TOC   "      F & D floating point : POLYD"
;13665
;13666 :      POLYD (75) ARG.RD, DEGREE.RW, TBLADDR.AB
;13667 :ENTER AT C.FORK WITH <RC 0, Q> HAVE ARG.RX, D HAS DEGREE.RW.
;13668 :WHEN DONE, <R0, R1> = RESULT, R2 = 0, R3 = TABLE ADDR + DEG*8 + 8,
;13669 :          R4 = 0, R5 = 0.
;13670 :IN PROCESSING, <R0, R1> = PARTIAL RESULT, R2 = DEG, R3 = NEXT TABLE ADDR,
;13671 :          <R4, R5> = ARG.
;13672 :
;13673
;13674 385:
;13675 POLYD: -----: D.D.OXT[WORD], GET DEGREE.RW
;13676 STATE_K[.1],J/POLYD.0 : SET POLYD FLAG
;13677 OC3:
;13678 POLYD.FPD:
;13679 -----:
;13680 D.R[R2],Q,0,SC_K[.FFF8], SETUP TO GET PC DELTA
;13681 J7FL.ABS.T014
;13682
;13683 1014:           :ASSIGN THIS ADD BECAUSE PCS CALLS IT
;13684 FL.ABS.1014:
;13685 -----: D_DAL.SC : PC DELTA IN D[07:00]
;13686
;13687
;13688 =00 :00-----: PC&VA_D.OXT[BYTE]+PC, BYPASS SPECIFIERS
;13689 CALL, J/SETFPD : MUST ESTABLISH A VALID FPD ERROR HANDLER!
;13690
;13691 =10 :10-----: MEM MGMT CODE COMES HERE ON READ ERRORS
;13692 Q_PC, J/BAKUP.PC : BACK UP PC AND CAUSE EXCEPTION
;13693
;13694
;13695
;13696 =:END :11-----: SETFPD RETURNS HERE
;13697 VA_R[R3], J/POLYD.9 : GET TABLE ADDR, JUMP BACK INTO LOOP
  
```

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204]  
; P1W124.MCR 600,1204] MICRO2 1L(03) F & D floating point : POLYD

I 12  
F & D floating point : POLYD 14-Jan-82 14-Jan-82 15:30:16

Fiche 2 Frame I12 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124

Sequence 357 Page 356

: FLOAT .MIC [600,1204]

U 1013, 0019,0024,8D80,F900,0010,13F6 : 13698 1013: :ASSIGN THIS ADDRESS BECAUSE PCS CALLS IT  
: 13699 POLYD.0:-----  
: 13700 LC RC[T0], : LATCH ARG <H>  
: 13701 ALU\_D.ANDNOT.K[.1F], : CHECK IF DEGREE > 31  
: 13702 CLK.UBCC : CLOCK IN ALU.Z  
: 13703  
: 13704 :-----  
: 13705 ID[T0] D, : SAVE DEGREE  
: 13706 D LC.CRK.FLT.CPR, : CHECK ARG.RX FOR -0  
: 13707 SC LC(EXP) : ARG EXP  
: 13708 INTRPT.STROBE, Z? : DEGREE > 31?  
: 13709  
: 13710 =01\*\*\*\*0;0-----: DEGREE > 31  
: 13711 J/RSVOPR : RESERVED OPERAND  
: 13712 :-----  
: 13713 1-----: DEGREE IN RANGE OF 0 TO 31.  
: 13714 ID[T2] D,FE\_SC, : T2 SAVES ARG <H>, FE SAVES ARG EXP  
: 13715 RC[T2] Q, : RC 2 SAVES ARG <L>  
: 13716 CALL,INTERRUPT.REQ?, :  
: 13717 J/ASPC : GO GET TABLE ADDR  
: 13718  
: 13719 =11\*\*\*\*1:-----: ASPC ALWAYS RETURNS 60 IN THIS CASE  
: 13720 R[R15] D, : SAVE TABLE ADDR  
: 13721 D[LONG]\_CACHE : GET 1ST COEF  
: =:END  
: 13722  
: 13723  
: 13724  
: 13725 ID[T1]\_D.LAB\_R[R15], :  
: 13726 ALU\_D.CHK.F[T.OPR, : TEST CO FOR RESERVED OP BEFORE SETTING FPD  
: 13727 VA\_VA+4 :  
: 13728  
: 13729 =00 :00-----  
: 13730 D[LONG] CACHE, : CO <L>  
: 13731 LC RC[T0], : LATCH ARG <H>  
: 13732 CALL,J/SETFPD :  
: 13733  
: 13734 =10 :10-----  
: 13735 Q\_PC, J/BAKUP.PC : READ ERR  
: 13736 BACK UP PC AND CAUSE EXCEPTION  
: 13737  
: 13738 ID[T4] D, :  
: 13739 R[R4]\_C : SAVE CO <L>  
: 13740 =:END : R4 STORES ARG <H>  
: 13741  
: 13742 R[R3]\_LA : R3 GETS TABLE ADDR

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 J 12  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Sequence 358  
 : FLOAT .MIC [600,1204] F & D floating point : POLYD

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	:13743 =0	-----;	
	:13744 ALU 0(A),	; CLR RUNNING PROD <L>	
	:13745 LC R <sub>C</sub> [T2]&R <sub>1</sub> .ALU,	; LATCH ARG <L>	
	:13746 CAEL,J/POLY.PC	; GOTO GET PC DELTA	
	:13747		
	:13748		
	:13749 SC FE,	; SC GETS BACK ARG EXP	
U 1238, 0003,003D,0180,FB90,0000,13E8	:13750 R[R2]_D.OR.Q	; R2 STORES PC DELTA, DEGREE	
	:13751 =;END		
	:13752		
	:13753 R[R5]_LC,	; RS STORES ARG <L>	
U 13FA, 0010,0038,C5F0,2EA8,0000,13FB	:13754 Q_ID[T1]	; GET CO <H>	
	:13755		
	:13756		
U 13FB, 0C01,203C,C1F0,2C00,0118,73FC	:13757 FE_Q(EXP).CLK.UBLCS.	; FE GETS CO EXP	
	:13758 D_Q,Q_ID[T0]	; GET BACK DEGREE	
	:13759		
	:13760		
U 13FC, 0C01,003C,D1F0,2E80,0000,13FE	:13761 R[R0]_D,	; RO STORES CO <1>	
	:13762 D_Q,Q_ID[T4]	; D GETS DEGREE, Q GETS CO <L>	
	:13763		
	:13764		
U 13FE, 0101,203C,0180,FA88,0000,140E	:13765 R[R1]_Q,	; STORE CO <L> AS RUNNING SUM <L>	
	:13766 D_D.LEFT[2].SI/ZERO	; DEGREE * 4	
	:13767		
	:13768		
	:13769 R[R3]&VA_LA+K[.8],	; SET UP TABLE ADDR IN R3, VA	
	:13770 D_D.LEFT_SI/ZERO,	; DEGREE * 8	
U 140E, 0518,0D14,0187,FA98,0200,1074	:13771 SGN/CLR.SD+SS,	; CLEAR SS FOR EALU BRANCH	
	:13772 D.NE.0?	; DEGREE .NE. 0?	
	:13773		
	:13774 =10*	0-----;	DEGREE .EQ. 0
U 1074, 0000,123C,0180,F800,0000,1092	:13775 EALU.Z?,J/POLYD.4	; IS CO = 0?	
	:13776		
U 1076, 0000,143C,0180,F800,0000,1351	:13777	1-----;	DEGREE > 0
	:13778 SC.GT.0?	; ARG = 0?	
	:13779 =;END		
	:13780		
U 1351, 001C,2014,0180,FA98,0200,1412	:13781 :0-----;	ARG = 0	
	:13782 R[R3]_LA+D, VA_ALU,	; ADVANCE STATE TO LAST COEFFICIENT	
	:13783 J/POLYD.8		
	:13784		
	:13785		
U 1353, 0800,003C,0180,FA20,0000,1413	:13786 :1-----;	ARG .NE. 0	
	:13787 D_R[R4],J/POLYD.10	; ARG <H>	
	:13788 =;END		
	:13789		
	:13790		

```

:13789 =*01*
:13790 POLYD.4:0-----: C0 .NE. 0
:13791 R[R4]_0, J/POLYD.35 : CLEAR R4, GO CLR R5 & R2 & EXIT
:13792
:13793 :1-----: C0 .EQ. 0
:13794 R[R0]_0 : ZERO RESULT<H>
:13795
:13796 :-----: ZERC RESULT<L> AND GO CLEAN UP
:13797 R[R1]_0, J/POLYD.4 : 
:13798
:13799
:13800 POLYD.8:-----: CONTINUATION OF ARG=0 SPECIAL CASE CODE
:13801 R[R2]_K[.1], DT/BYTE : TABLE ADDR & DEGREE NOW INDICATE LAST COEF
:13802 :-----: FALL INTO MAIN LOOP FOR 1 ITERATION
:13803
:13804 :-----: POLYD LOOP BEGINS HERE
:13805
:13806
:13807 =110 POLYD.9:0-----: NO: NO INTERRUPTS
:13808 D_R[R4].J/POLYD.10 : ARG <H>
:13809
:13810 :1-----: YES: INTERRUPTS
:13811 J/POLY.INT : INTERRUPT ENTRY TO CLR TP AND BACKUP PC,R'S
=:END
:13812
:13813
:13814 POLYD.10:-----: 
:13815 R[C[T0]]_D : ARG <H>
:13816
:13817
:13818 Q_R[R5] : ARG <L>
:13819
  
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ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 L 12  
 : F1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, F<sup>0</sup>LA 0E, WCS124 Sequence 360  
 ; FLOAT .MIC [600,1204] F & D floating point : POLYD Page 359

U 1422, 0800,003C,0180,FA00,0000,1423	:13820		
	:13821	D_R[0]	PART PROD <H>
	:13822		
	:13823		
U 1423, 0001,003C,0580,FB08,1404,7280	:13824	ALU_D, STATE K[.1],	SET POLYD FLAG FOR MULD
	:13825	LAB_R1&RC[T1]_ALU	RC 1 GETS PARTIAL PROD <H>
	:13826		
	=0**00		
	:13827	D_Q, SC_K[.10],	D GETS PROD <L>
	:13828	RC[T6]_LA,	SETUP FOR MULD
	:13829	CALL,J7MULD.02	CALL MULD RTN WITH STATE=1 AS FLAG
U 1280, 0C00,003D,6580,F9B0,0084,72C8	:13830		
	:13831		
U 1290, 0000,003C,0180,4218,0000,142A	:13832	=1**00 :00	PARTIAL PROD = 0
	:13833	D[LONG]_CACHE,	GET NEXT COEF <H>
	:13834	LAB_R[R3],	LATCH TABLE ADDR
	:13835	J/POLYD.12	
	:13836		
U 1292, 051B,0014,0428,F800,0084,B293	:13837	=1**10 :10	.25 <= PARTIAL PROD FRACT < .5
	:13838	ALU_0+K[.1], Q_Q.LEFT,	SHIFT FRACTION 1 BIT TO THE LEFT
	:13839	D_D.LEFT, SI7DIVD,	
	:13840	SC_SC-K[.1]	AND ADJUST EXPONENT TO MATCH
	:13841		
	:13842	:11-----	.5 <= PARTIAL PROD FRACT <1.0
	:13843	ID[T0]_D, RC[T3]_D,	SAVE PROD FRACT <H>
	:13844	D_Q, Q_D,	SWAP HALVES SO WE CAN SAVE LO PART
	:13845	F_E SC,	SAVE EXP
U 1293, 0C01,143C,C1E0,3D98,0100,1371	:13846	SC?, J/POLYD.13	TEST FOR MULTIPLY OVERFLOW
	:13847	=;END	
	:13848		
	:13849	POLYD.12:-----	PARTIAL PROD = 0
	:13850	ALU_D, Q_ALU,	MOVE RESULT<H> TO Q THRU ALU
	:13851	CHK_FLT_OPR,	CHECK FOR -0
	:13852	EALU_D(EXP),CLK.LBCC,	CHECK FOR EXP 0
	:13853	SGN/CLR_SD+SS,	CLEAR SS FOR EALU BRANCH
	:13854	VA_VA+4	INCREMENT TABLE ADDR
U 142A, 0001,003C,01C7,F803,0818,742B	:13855		
U 142B, 0000,003C,0180,4000,0000,142C	:13856	D[LONG]_CACHE	RESULT <L> - DON'T BUMP R3 HERE, MAY FAULT
U 142C, 0018,1214,0180,FA98,0000,10EA	:13857		
	:13858		
	:13859		
	:13860	R[R3]_LA+K[.8],	INCREMENT TABLE ADDR TO POINT TO NEXT COEF
	:13861	EALU.Z?	RESULT = 0?
	:13862		
	:13863	=*01* :0-----	NOT 0
U 10EA, 0001,003C,0180,FA88,0000,1253	:13864	R[R1]_D,	STORE RESULT <L>
	:13865	J/POLYD.21	GO STORE RESULT <H>
	:13866		
	:13867	:1-----	RESULT 0
	:13868	R[R0]_0, Q_0, D_0,	RESULT IS A TRUE 0
	:13869	J/POLYD.21	
U 10EE, 0F03,003C,01F8,FA80,0000,1253	:13870	=;END	
	:13871		

ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Sequence 361  
 ; FLOAT .MIC [600,1204] F & D floating point : POLYD Page 360

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Sequence 361

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	:13872 =001	; TEST FOR MULTIPLY OVERFLOW
	:13873 POLYD.13:;00-----	PARTIAL PROD .NE. 0, EXP = 0
	:13874 ID[T2]_D, ALU_Q,	SAVE PROD FRAC<L>
	:13875 D_ALU_LEFT, SI/ZERO,	PUT PROD FRAC<H> IN D NORMALIZED
	:13876 [AB_R[R3]], J/POLYD.14	LATCH COEF TABLE ADDRESS
	:13877	
	:13878 :01-----	PROD .NE. 0, 0 < EXP < 100
	:13879 ID[T2]_D, ALU_Q,	SAVE PROD FRAC<L>
	:13880 D_ALU_LEFT, SI/ZERO,	PUT PROD FRAC<H> IN D NORMALIZED
	:13881 [AB_R[R3]], J/POLYD.14	LATCH COEF TABLE ADDRESS
	:13882	
	:13883 :10-----	PROD .NE. 0, EXP < 0
	:13884 ID[T2]_D, ALU_Q,	SAVE PROD FRAC<L>
	:13885 D_ALU_LEFT, SI/ZERO,	PUT PROD FRAC<H> IN D NORMALIZED
	:13886 [AB_R[R3]], J/POLYD.14	LATCH COEF TABLE ADDRESS
	:13887	
	:13888 :11-----	PROD .NE. 0, EXP > 100 (OVERFLOW)
	:13889 STATE_K[.20], J/POLYD.13	SET FLAG SAYING THAT PRODUCT OVERFLOWED.
	:13890	THIS FLAG IS NECESSARY BECAUSE ADDD
	:13891	WILL LOSE TRACK OF THE 9TH EXPONENT BIT
	:13892	DURING ITS CALCULATIONS (SIGH)
	:13893	
	:13894 POLYD.14:;-----	
	:13895 EALU_FE,RC[T0]_PACK.FP,	SAVE PACKED PROD<H>, IGNORING POSS. UNDRFLOW
	:13896 D[LONG]_CACHE	READ NEXT COEF<H>
	:13897	
	:13898	
	:13899 RC[T1]_D, CHK.FLT.OPR,	CHECK FOR -0
	:13900 Q_D, VA_VA+4	INCREMENT TABLE ADDR
	:13901	
	:13902	
	:13903 D[LONG]_CACHE	READ COEF<L> - DON'T BUMP R3 YET, MAY FAULT
	:13904	
	:13905	
	:13906 R[R3]_LA+K[.8]	INCREMENT TABLE ADDR
	:13907	
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ZZ-ES0AA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 0i, FPLA 0E, WCS124  
 : FLOAT .MIC [600,1204] F & D floating point : POLYD

N 12

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Sequence 362

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	:13907 =00	:00-----	; CALL CONSTRAINT BLOCK
U 1358, 0001,003D,0580,F980,1404,288E	:13908	STATE STATE.OR.K[1],	; SET POLYD FLAG AGAIN FOR ADDD
	:13909	RC[T6]_D,CALL,J/UNPK	; SAVE COEF<L> AND UNPACK COEF.
	:13910		
	:13911	:01-----	; IT IS 0
U 1359, 0000,003C,C9F4,2C00,0000,1433	:13912	SD_SS,0_ID[T2],	; PROD <L>
	:13913	J/POLYD.16	
	:13914		
	:13915	:1-----	; NOT 0
U 135A, 0018,0038,1D80,FAF8,0190,B241	:13916	R[R15] K[SC],	; SAVE SC WHILE WE COMPUTE EXP DIFF
	:13917	FS SC-FE,SC_SC-FE,	; GET EXPONENT DIFFERENCE
	:13918	CLR.UBCC	; FOR COMPARE EXP'S
	:13919	=	
	:13920		
U 1241, 001B,1401,1D80,FA78,0082,1395	:13921	=0*001 :0*001-----	; CALL SITE FOR ADDD
	:13922	ALU_0-K[SC],SC_ALU,	; GET NEG OF EXP DIFF IN CASE ITS POS
	:13923	LAB_R[R15]	; LATCH SAVED SC FOR RELOADING
	:13924	SC.GT.0?,CALL[POLYD.A]	; GO ADD, NEGATING EXP DIFF IF IT IS POS
	:13925		
	:13926		
	:13927		
U 1251, 0000,163C,0180,F800,0000,10B5	:13928	=1*001 :1*001-----	; SC.eq.0, UNDERFLOW OR OVERFLOW
	:13929	STATE5?,J/POLYD.15	; DEPENDING ON OV FLAG
	:13930		
	:13931	POLYD.21:	
U 1253, 0000,163C,0180,F800,0000,123C	:13932	:1*011-----	; SC.eq.[01 to FF], OK OR OVERFLOW
	:13933	STATE5?,J/POLYD.17	; OVERFLOW, DEPENDING ON OV FLAG
	:13934		
U 1255, 0000,163C,0180,F800,0000,10B1	:13935	:1*101-----	; SC.lss.0, UNDERFLOW OR OK
	:13936	STATE5?,J/POLYD.24	; UNDERFLOW OR OK, DEPENDING ON OV FLAG
	:13937		
U 1257, 0818,0038,0180,FA18,0000,13F1	:13938	:1*111-----	; SC.gt.FF, OVERFLOW
	:13939	D_K[.8],	; D GETS OVERFLOW TRAP CODE
	:13940	LAB_R[R3],J/POLYDFAULT	; FETCH TABLE ADDRESS

U 1395, 0000,123C,C9F0,2D08,0082,0182

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:13941 =101
:13942 POLYD.A:;101-----; SUBR TO TALK TO ADDD - EXP DIFF <=0 ENTRY
:13943   LC RC[T1], SC_LA, : LATCH PACKED COEF<H>, SET EXP = DST EXP,
:13944   Q_ID[T2],          : PUT PROD<L> IN Q WHERE ADDD EXPECTS IT
:13945   EALU?, J/ADDD.10   : DISPATCH INTO THE ADDD ROUTINE
:13946
:13947   ;1-----; EXP DIFF > 0 ENTRY
:13948   LC RC[T1], SC_LA, : LATCH PACKED COEF<H>, SET EXP=DST EXP,
:13949   Q_ID[T2],          : PUT PROD<L> IN Q WHERE ADDD EXPECTS IT
:13950   FE_SC, EALU?, J/ADDD.10 : NEGATE DIFF & DISPATCH INTO THE ADDD ROUTINE
:13951
:13952
:13953 POLYD.16:;-----; COME HERE WHEN COEFFICIENT = 0
:13954   D_Q,Q_RC[T3].      : SET FOR PACKING DOUBLE RESULT
:13955   ST_FE.              : SC GETS EXP
:13956   FE_K[.18]           : SET 24. FOR PACKING DOUBLE RESULT
:13957
:13958
:13959   D_D.LEFT,Q_Q.LEFT. : DOUBLE SHIFT <Q,D>
:13960   SI/ASHL,K[.80]
:13961
:13962 =00001 ;00001-----; ** THIS CONSTRAINT USED FOR MANY THINGS
:13963   D_Q,Q_D+K[.80].    : RESULT FRACS IN <D,Q>
:13964   C[K.UBCC.          : CHECK IF CARRY
:13965   CALL,J/PACKD       : CALL PACK SUBRT
:13966 =10001
:13967 POLYD.24:
:13968   ;10001-----; RESULT UNDERFLOW
:13969   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13970
:13971   ;10011-----; RESULT OK
:13972   R[R0]_Q_Q_D,J/POLYD.22 ; STORE RESULT <H>. Q GETS RESULT <L>
:13973
:13974
:13975 POLYD.15:
:13976   ;10101-----; RESULT UNDERFLOW
:13977   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13978
:13979   ;10111-----; RESULT OVERFLOW
:13980   D_K[.8],          : D GETS OVERFLOW TRAP CODE
:13981   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
:13982
:13983 =11101 ;11101-----; RETURN HERE IF PSL<fu>.eq.0(SC.eq.0)
:13984   R[R0]_Q_STATE_K[ZERO],Q_0. ; PRETEND IT DIDN'T HAPPEN
:13985   J/POLYD.22
:13986
:13987   ;11111-----; RETURN HERE IF PSL<fu>.eq.1(SC.ne.0)
:13988   D_K[.A],          : D GETS UNDERFLOW TRAP CODE
:13989   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
  
```

U 1433, 0C10,0038,7DC0,F918,0185,7438

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:13954   D_Q,Q_RC[T3].      : SET FOR PACKING DOUBLE RESULT
:13955   ST_FE.              : SC GETS EXP
:13956   FE_K[.18]           : SET 24. FOR PACKING DOUBLE RESULT
:13957
:13958
:13959   D_D.LEFT,Q_Q.LEFT. : DOUBLE SHIFT <Q,D>
:13960   SI/ASHL,K[.80]
:13961
:13962 =00001 ;00001-----; ** THIS CONSTRAINT USED FOR MANY THINGS
:13963   D_Q,Q_D+K[.80].    : RESULT FRACS IN <D,Q>
:13964   C[K.UBCC.          : CHECK IF CARRY
:13965   CALL,J/PACKD       : CALL PACK SUBRT
:13966 =10001
:13967 POLYD.24:
:13968   ;10001-----; RESULT UNDERFLOW
:13969   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13970
:13971   ;10011-----; RESULT OK
:13972   R[R0]_Q_Q_D,J/POLYD.22 ; STORE RESULT <H>. Q GETS RESULT <L>
:13973
:13974
:13975 POLYD.15:
:13976   ;10101-----; RESULT UNDERFLOW
:13977   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13978
:13979   ;10111-----; RESULT OVERFLOW
:13980   D_K[.8],          : D GETS OVERFLOW TRAP CODE
:13981   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
:13982
:13983 =11101 ;11101-----; RETURN HERE IF PSL<fu>.eq.0(SC.eq.0)
:13984   R[R0]_Q_STATE_K[ZERO],Q_0. ; PRETEND IT DIDN'T HAPPEN
:13985   J/POLYD.22
:13986
:13987   ;11111-----; RETURN HERE IF PSL<fu>.eq.1(SC.ne.0)
:13988   D_K[.A],          : D GETS UNDERFLOW TRAP CODE
:13989   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
  
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U 1438, 0500,003C,4128,F800,0000,10A1

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:13959   D_D.LEFT,Q_Q.LEFT. : DOUBLE SHIFT <Q,D>
:13960   SI/ASHL,K[.80]
:13961
:13962 =00001 ;00001-----; ** THIS CONSTRAINT USED FOR MANY THINGS
:13963   D_Q,Q_D+K[.80].    : RESULT FRACS IN <D,Q>
:13964   C[K.UBCC.          : CHECK IF CARRY
:13965   CALL,J/PACKD       : CALL PACK SUBRT
:13966 =10001
:13967 POLYD.24:
:13968   ;10001-----; RESULT UNDERFLOW
:13969   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13970
:13971   ;10011-----; RESULT OK
:13972   R[R0]_Q_Q_D,J/POLYD.22 ; STORE RESULT <H>. Q GETS RESULT <L>
:13973
:13974
:13975 POLYD.15:
:13976   ;10101-----; RESULT UNDERFLOW
:13977   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13978
:13979   ;10111-----; RESULT OVERFLOW
:13980   D_K[.8],          : D GETS OVERFLOW TRAP CODE
:13981   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
:13982
:13983 =11101 ;11101-----; RETURN HERE IF PSL<fu>.eq.0(SC.eq.0)
:13984   R[R0]_Q_STATE_K[ZERO],Q_0. ; PRETEND IT DIDN'T HAPPEN
:13985   J/POLYD.22
:13986
:13987   ;11111-----; RETURN HERE IF PSL<fu>.eq.1(SC.ne.0)
:13988   D_K[.A],          : D GETS UNDERFLOW TRAP CODE
:13989   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
  
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U 10A1, 0C19,0015,41C0,F800,0010,03FC

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:13963   D_Q,Q_D+K[.80].    : RESULT FRACS IN <D,Q>
:13964   C[K.UBCC.          : CHECK IF CARRY
:13965   CALL,J/PACKD       : CALL PACK SUBRT
:13966 =10001
:13967 POLYD.24:
:13968   ;10001-----; RESULT UNDERFLOW
:13969   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13970
:13971   ;10011-----; RESULT OK
:13972   R[R0]_Q_Q_D,J/POLYD.22 ; STORE RESULT <H>. Q GETS RESULT <L>
:13973
:13974
:13975 POLYD.15:
:13976   ;10101-----; RESULT UNDERFLOW
:13977   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13978
:13979   ;10111-----; RESULT OVERFLOW
:13980   D_K[.8],          : D GETS OVERFLOW TRAP CODE
:13981   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
:13982
:13983 =11101 ;11101-----; RETURN HERE IF PSL<fu>.eq.0(SC.eq.0)
:13984   R[R0]_Q_STATE_K[ZERO],Q_0. ; PRETEND IT DIDN'T HAPPEN
:13985   J/POLYD.22
:13986
:13987   ;11111-----; RETURN HERE IF PSL<fu>.eq.1(SC.ne.0)
:13988   D_K[.A],          : D GETS UNDERFLOW TRAP CODE
:13989   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
  
```

U 10B1, 0000,003D,3DF0,2C00,0000,12AE

```

:13969   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13970
:13971   ;10011-----; RESULT OK
:13972   R[R0]_Q_Q_D,J/POLYD.22 ; STORE RESULT <H>. Q GETS RESULT <L>
:13973
:13974
:13975 POLYD.15:
:13976   ;10101-----; RESULT UNDERFLOW
:13977   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13978
:13979   ;10111-----; RESULT OVERFLOW
:13980   D_K[.8],          : D GETS OVERFLOW TRAP CODE
:13981   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
:13982
:13983 =11101 ;11101-----; RETURN HERE IF PSL<fu>.eq.0(SC.eq.0)
:13984   R[R0]_Q_STATE_K[ZERO],Q_0. ; PRETEND IT DIDN'T HAPPEN
:13985   J/POLYD.22
:13986
:13987   ;11111-----; RETURN HERE IF PSL<fu>.eq.1(SC.ne.0)
:13988   D_K[.A],          : D GETS UNDERFLOW TRAP CODE
:13989   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
  
```

U 10B3, 0001,203C,01E0,FA80,0000,1439

```

:13971   ;10011-----; RESULT OK
:13972   R[R0]_Q_Q_D,J/POLYD.22 ; STORE RESULT <H>. Q GETS RESULT <L>
:13973
:13974
:13975 POLYD.15:
:13976   ;10101-----; RESULT UNDERFLOW
:13977   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13978
:13979   ;10111-----; RESULT OVERFLOW
:13980   D_K[.8],          : D GETS OVERFLOW TRAP CODE
:13981   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
:13982
:13983 =11101 ;11101-----; RETURN HERE IF PSL<fu>.eq.0(SC.eq.0)
:13984   R[R0]_Q_STATE_K[ZERO],Q_0. ; PRETEND IT DIDN'T HAPPEN
:13985   J/POLYD.22
:13986
:13987   ;11111-----; RETURN HERE IF PSL<fu>.eq.1(SC.ne.0)
:13988   D_K[.A],          : D GETS UNDERFLOW TRAP CODE
:13989   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
  
```

U 10B5, 0000,003D,3DF0,2C00,0000,12AE

```

:13971   ;10011-----; RESULT OK
:13972   R[R0]_Q_Q_D,J/POLYD.22 ; STORE RESULT <H>. Q GETS RESULT <L>
:13973
:13974
:13975 POLYD.15:
:13976   ;10101-----; RESULT UNDERFLOW
:13977   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13978
:13979   ;10111-----; RESULT OVERFLOW
:13980   D_K[.8],          : D GETS OVERFLOW TRAP CODE
:13981   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
:13982
:13983 =11101 ;11101-----; RETURN HERE IF PSL<fu>.eq.0(SC.eq.0)
:13984   R[R0]_Q_STATE_K[ZERO],Q_0. ; PRETEND IT DIDN'T HAPPEN
:13985   J/POLYD.22
:13986
:13987   ;11111-----; RETURN HERE IF PSL<fu>.eq.1(SC.ne.0)
:13988   D_K[.A],          : D GETS UNDERFLOW TRAP CODE
:13989   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
  
```

U 10B7, 0818,0038,0180,FA18,0000,13F1

```

:13971   ;10011-----; RESULT OK
:13972   R[R0]_Q_Q_D,J/POLYD.22 ; STORE RESULT <H>. Q GETS RESULT <L>
:13973
:13974
:13975 POLYD.15:
:13976   ;10101-----; RESULT UNDERFLOW
:13977   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13978
:13979   ;10111-----; RESULT OVERFLOW
:13980   D_K[.8],          : D GETS OVERFLOW TRAP CODE
:13981   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
:13982
:13983 =11101 ;11101-----; RETURN HERE IF PSL<fu>.eq.0(SC.eq.0)
:13984   R[R0]_Q_STATE_K[ZERO],Q_0. ; PRETEND IT DIDN'T HAPPEN
:13985   J/POLYD.22
:13986
:13987   ;11111-----; RETURN HERE IF PSL<fu>.eq.1(SC.ne.0)
:13988   D_K[.A],          : D GETS UNDERFLOW TRAP CODE
:13989   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
  
```

U 10BD, 0003,003C,19F8,FA80,1404,7439

```

:13971   ;10011-----; RESULT OK
:13972   R[R0]_Q_STATE_K[ZERO],Q_0. ; PRETEND IT DIDN'T HAPPEN
:13973
:13974
:13975 POLYD.15:
:13976   ;10101-----; RESULT UNDERFLOW
:13977   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13978
:13979   ;10111-----; RESULT OVERFLOW
:13980   D_K[.8],          : D GETS OVERFLOW TRAP CODE
:13981   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
:13982
:13983 =11101 ;11101-----; RETURN HERE IF PSL<fu>.eq.0(SC.eq.0)
:13984   R[R0]_Q_STATE_K[ZERO],Q_0. ; PRETEND IT DIDN'T HAPPEN
:13985   J/POLYD.22
:13986
:13987   ;11111-----; RETURN HERE IF PSL<fu>.eq.1(SC.ne.0)
:13988   D_K[.A],          : D GETS UNDERFLOW TRAP CODE
:13989   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
  
```

U 10BF, 0818,0038,F580,FA18,0000,13F1

```

:13971   ;10011-----; RESULT OK
:13972   R[R0]_Q_STATE_K[ZERO],Q_0. ; PRETEND IT DIDN'T HAPPEN
:13973
:13974
:13975 POLYD.15:
:13976   ;10101-----; RESULT UNDERFLOW
:13977   Q_ID[PSL],CALL[PSLFU.A] ; GO SEE IF PSL<fu> IS SET
:13978
:13979   ;10111-----; RESULT OVERFLOW
:13980   D_K[.8],          : D GETS OVERFLOW TRAP CODE
:13981   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
:13982
:13983 =11101 ;11101-----; RETURN HERE IF PSL<fu>.eq.0(SC.eq.0)
:13984   R[R0]_Q_STATE_K[ZERO],Q_0. ; PRETEND IT DIDN'T HAPPEN
:13985   J/POLYD.22
:13986
:13987   ;11111-----; RETURN HERE IF PSL<fu>.eq.1(SC.ne.0)
:13988   D_K[.A],          : D GETS UNDERFLOW TRAP CODE
:13989   LAB_R[R3],J/POLYDFAULT ; FETCH TABLE ADDRESS
  
```

ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] ; P1W124.MCR 600,1204] ; FLOAT .MIC [600,1204] C 13  
 : MICRO2 1L(03) 14-Jan-82 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 : F & D floating point : POLYD Fiche 2 Frame C13 Sequence 364  
 Page 363

```

:13989 =**0*
:13990 POLYD.17:
:13991 ;**0-----;
:13992 R[R0] Q, Q, D, ; BRANCH CONSTRAINT FOR STATE<5>
:13993 STATE_K[ZER0],J/POLYD.22 ; SAVE HIGH RESULT, Q GETS LO RESULT
:13994 ;-----;
:13995 ;-----;
:13996 D,[.8], ; CLEAR ALL FLAGS
:13997 LAB_R[R3],J/POLYDFAULT ; D GETS OVERFLOW TRAP CODE
:13998 ;-----; ; FETCH TABLE ADDRESS
:13999 POLYD.22:
:14000 ;-----;
:14001 LAB_R[R2] ;-----;
:14002 ;-----;
:14003 ;-----;
:14004 ;-----;
:14005 VA VA+4, ;-----;
:14006 R[R2] LA-K[.1],DT/BYTE, ; INR COEF ADDR
:14007 CLK.U8CC ; DECREMENT DEGREE COUNT
:14008 ;-----;
:14009 ;-----;
:14010 R[R1]_Q,INTRPT.STROBE,Z? ; SET Z IF WE ARE DONE
:14011 ;-----;
:14012 =0 ;0-----; ; STORE RESULT<L>, ENABLE INT, DONE?
:14013 INTERRUPT.REQ?,J/POLYD.9 ; NO:
:14014 ;-----; ; GOTO NEXT LOOP
:14015 ;1-----; ; YES:
:14016 R[R4]_K[ZERO] ; CLR R4 (ARG <H>)
:14017 ;-----;
:14018 POLYD.35:
:14019 ;-----;
:14020 CLR.FPD,R[R5]_K[ZERO] ; CLR PSL <FPD> AND ARG<L>
:14021 ;-----;
:14022 ;-----;
:14023 R[R2]_K[ZERO], ; CLR DEGREE--UNDERFLOW FLAG--PC DELTA
:14024 SC_FE ; GET BACK EXP
:14025 SUB/SPEC,J/POLY.C ; GOTO SET COND CODES
:14026 ;-----;
:14027 .REGION/0000,0FFF ;Lower 4k for PCS
  
```

0 13  
ZZ-ESOAA-124.0 ; FLOAT .MIC [600,1204] F & D floating point 14-Jan-82 Fiche 2 Frame D13 Sequence 365  
; P1WT24.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 364  
; FLOAT .MIC [600,1204] F & D floating point : POLYD

14027; This page intentionally left blank.

ZZ-ES0AA-124.0 : INIT2 .MIC [600,1204] INIT2.MIC E 13  
: P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 Fiche 2 Frame E13 Sequence 366  
: INIT2 .MIC [600,1204] INIT2.MIC VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 365

:14028 .TOC "'INIT2.MIC'"  
:14029 .TOC "Revision 0.2"  
:14030 : P. R. Guilbault  
:14031

:14032 .NOBIN ..  
:14033 .TOC .. Revision History"  
:14034 ..  
:14035 : 00 Start of history  
:14036

:14037 .BIN  
:14038 .NOLIST ;Disable listing of PCS code for quickie assemblies

ZZ-ESOAA-124.0 ; INIT2 .MIC [600,1204] Initialize microcod F 13  
 ; P1WT24.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124  
 ; INIT2 .MIC [600,1204] Initialize microcode :INITIALIZE MACHINE ROUTINE

Fiche 2 Frame F13 Sequence 367  
 Page 366

```

;14039 .TOC " Initialize microcode :INITIALIZE MACHINE ROUTINE"
;14040
;14041 ;***** *****
;14042 *
;14043 * INITIALIZE MACHINE *
;14044 *
;14045 ;***** *****
;14046
;14047 ;THIS ROUTINE IS USED TO INITIALIZE THE REQUIRED ID-REGISTERS,
;14048 ;TBUF, CACHE, AND OPTIONAL ACCELERATOR. AFTER COMPLETING THESE
;14049 ;TASKS, THIS ROUTINE ENTERS A WAIT LOOP, WAITING FOR
;14050 ;THE CONSOLE TO INITIATE EITHER A WARM START OR COLD START
;14051 ;PROCEDURE.
;14052
;14053 ;INITIALIZE ID REGISTERS
;14054
;14055 100:
;14056 SYS.INIT:
;14057 -----
;14058 SC_K[.F], 15 TO SC TO CONSTRUCT BIT MASK
;14059 STOP.IB, MCT/MEM.NOP : STOP IBUFFER
;14060 : CONSOLE MODE SET, SO IF ERROR GO TO IT
;14061
;14062 -----
;14063 D NOT.MASK, 0_0, : A '1' TO D<15> POSITION
;14064 SC_K[.6] : SETUP SC FOR LEFT SHIFT OF 6
;14065
;14066 -----
;14067 D_DAL.SC : SHIFT A '1' BIT INTO POS<21>
;14068
;14069 =0100* :0100-----
;14070 ID[MAINT].D, : SET SBI ENABLE INVALIDATE BIT
;14071 CALL, J/WPR.10A : GO AND CLEAR TBUF

```

U 010J, 1000,003C,6180,0800,0084,6984

U 0984, 0803,001C,D5F8,F800,0084,6985

U 0985, 0D00,003C,0180,F800,0000,01E8

U 01E8, 0000,003D,7580,3C00,0000,08D0

ZZ-ESOAA-124.0 : INIT2 .MIC [600,1204] Initialize microcod G 13  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Sequence 368  
 : INIT2 .MIC [600,1204] Initialize microcode :INITIALIZE MACHINE ROUTINE Page 367

```

:14072      ;*****  

:14073      ;  

:14074      ;CLEAR CACHE ROUTINE *  

:14075      ;  

:14076      ;*****  

:14077      ;  

:14078      ;THIS ROUTINE IS USED TO RESET THE CONTENTS OF CACHE.  

:14079      ;THIS IS DONE BY ISSUING THE INVALIDATE CACHE MICRO ORDER  

:14080      ;TO EACH AND EVERY CACHE TAG LOCATION (1024). BOTH  

:14081      ;GROUPS, G0 & G1, ARE RESET TOGETHER.  

:14082      ;  

:14083      =1100* :1100*-----:  

:14084      SC_K[ZERO], D_0,      : CLEAR SC AND D-REGS  

:14085      VA_K[ZERO],          : INITIALIZE VA TO ZERO  

:14086      J/I.CACHE.5        : GO & WRITE INVALIDATES  

:14087      =  

:14088      =011  

:14089      I.CACHE.3:  

:14090      :011-----: *** LOOP FINISHED ***  

:14091      D_0,                : CLEAR D-REG  

:14092      Q_ID[ACC,CS],       : GET ACCELERATOR'S CONTROL/STATUS REG  

:14093      J7CLR.ACC          :  

:14094      ;  

:14095      I.CACHE.5:  

:14096      :111-----: *** CONTINUE LOOP ***  

:14097      CACHE.INVALIDATE,   : INVALIDATE G0 & G1 TAG ADDRESSED BY VA  

:14098      SC_SC+1             : INCREMENT COUNT  

:14099      ;  

:14100      ;  

:14101      VA_VA+4,            : INCREMENT  

:14102      SC_NE.0?,J/I.CACHE.3 : CHECK TO SEE IF ALL 1024 WRITTEN
  
```

```

;14103 ;*****  

;14104 *  

;14105 : RESET ACCELERATOR ROUTINE *  

;14106 *  

;14107 ;*****  

;14108 ;THIS ROUTINE CHECK TO SEE IF AN OPTIONAL ACCELERATOR  

;14109 ;IS ON THIS MACHINE, AND IF SO ISSUES A RESET TO  

;14110 ;IT. IT THEN WAITS UNTIL THE ACCELERATOR ISSUES AN ACCELERATOR  

;14111 ;SYNC, INDICATING THAT THE ACCELERATOR HAS INITIALIZED ITSELF.  

;14112 ;THE ACCELERATOR CONTROL AND STATUS REGISTER IS ALSO RESET.  

;14113  

;14114  

;14115 CLR.ACC:  

;14116 -----:  

;14117 ALU.Q.AND.K[F], : TEST TO SEE IF THERE IS AN ACCELERATOR  

;14118 CLK.UBCC : CLOCK ALU<Z> FOR TEST  

;14119  

;14120 -----:  

;14121 !D[ACC.CS]_D, : RESET ACCELERATOR'S CONTROL & STATUS REG  

;14122 Z? : IS AN ACCELERATOR ATTACHED?  

;14123  

;14124 =0 :0-----: *** ACCELERATOR IS INSTALLED ***  

;14125 TRAP.ACC[1], : TRAP ACCELERATOR TO ITS INITIALIZATION  

;14126 J/I.ACC.05 : ROUTINE  

;14127  

;14128 ;1-----: *** NO ACCELERATOR ****  

;14129 J/I.ACC.07 :  

;14130 =110 I.ACC.05:  

;14131 :110-----: *** NO ***  

;14132 D_K[.8000], : SETUP ENABLE BIT FOR ACCEL  

;14133 ACC.SYNC?, J/I.ACC.05 : HAS ACCELERATOR INITIALIZED ITSELF?  

;14134  

;14135  

;14136 :111-----: *** YES ***  

;14137 IDE[ACC.CS]_D : ENABLE ACCELERATOR

```

ZZ-ESOAA-124.0 ; INIT2 .MIC [600,1204] I 13  
 : P1W124.MCR 600,1204] MICRO2 1L(03) Initialize microcod14-Jan-82 Fiche 2 Frame I13 Sequence 370  
 : INIT2 .MIC [600,1204] Initialize microcode :INITIALIZE MACHINE ROUTINE VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 369

```

U 098A, 0818,0038,1180,F800,0000,098C   ;14138 I.ACC.07:-----;  

                                         ;14139 D_K[.4]           ; VALUE TO SET ASTLVL  

                                         ;14140  

U 098C, 0000,003C,3180,3C00,0000,098E   ;14141 -----;  

                                         ;14142 IDECES_D          ; SET ASTLVL TO 4  

                                         ;14143  

U 098E, 0818,0038,9180,F800,0000,0994   ;14144 -----;  

                                         ;14145 D_K[.1FO0]        ; GET 1F TO SET IPL TO 31  

                                         ;14146  

U 0994, 0819,0014,1180,F800,0000,0996   ;14147 -----;  

                                         ;14148 D_D+K[.4]         ; BIT TO SET 'IS'  

                                         ;14149  

                                         ;14150 -----;  

U 0996, 0818,0038,1980,F801,0200,0998   ;14151 D_D.SWAP          ; FINISH SETUP OF NEW PSL  

                                         ;14152 PC&VA_K[ZERO]     ; RESET PC TO ZERO  

                                         ;14153  

U 0998, 0000,003C,3D80,3C00,0000,0999   ;14154 -----;  

                                         ;14155 IDEPSL_D          ; SET IPL=31 AND IS=1  

                                         ;14156  

                                         ;14157 -----;  

                                         ;14158 :SETUP CONSTANT FOR MASKING OUT PTE MBZ FIELD IN GETPTE ROUTINE  

                                         ;14159  

U 0999, 081B,001C,9980,F800,0000,099C   ;14160 D_NOT.K[.E003]      ; GET CONSTANT FOR PTE MBZ FIELD  

                                         ;14161  

U 099C, 0800,003C,0180,F800,0000,099E   ;14162 -----;  

                                         ;14163 D_D.SWAP          ; ALIGN CONSTANT WITH MBZ FIELD  

                                         ;14164  

U 099E, 0001,003C,0180,F9F8,0000,09A0   ;14165 RCEPTE.MASK]_D     ; SETUP AND LEAVE IN RC REG FOR LATER USE  

                                         ;14166  

                                         ;14167  

                                         ;14168  

U 09A0, 0818,0038,0D80,F800,0000,039F   ;14169 D_K[.3],          ; WARM/COLD START CODE TO D-REG  

                                         ;14170 J7HALT.ERR        ; HALT MACHINE  

                                         ;14171  

                                         ;14172 .LIST           ;Re-enable full listing
  
```

ZZ-ES0AA-124.0 : INIT2 .MIC [600,1204] Initialize microcod J 13  
: P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Sequence 371  
; INIT2 .MIC [600,1204] Initialize microcode :INITIALIZE MACHINE ROUTINE Page 370

14172: This page intentionally left blank.

ZZ-ESOAA-124.0 : ASPC .MIC [600,1204] ASPC.MIC 14-Jan-82 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 K 13 Fiche 2 Frame K13 Sequence 372  
: P1W124.MCR 600,1204] MICRO2 IL(03) ASPC.MIC Page 371  
: ASPC .MIC [600,1204]

:14173 .TOC "ASPC.MIC"  
:14174 .TOC "Revision 1.1"  
:14175 : P. R. Guilbault  
:14176

:14177 .NOBIN ..  
:14178 .TOC .. Revision History"  
:14179  
:14180 : 01 Remove absolute jumps.  
:14181 : 00 Start of history  
:14182

:14183 .BIN  
:14184 .NOLIST ;Disable listing of PCS code for quickie assemblies

ZZ-ES0AA-124.0 ; ASPC .MIC [600,1204]  
; P1W124.MCR 600,1204]  
; ASPC .MIC [600,1204]

.MIC [600,1204] I-stream decode for 14-Jan-82  
MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124  
I-stream decode forks : Address Specifier Evaluation

L 13

Fiche 2 Frame L13

Sequence 373

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U 047E, F000,003F,01F0,F847,0000,0400

U 0400, 0000,003C,0180,F800,0000,0001

U 0401, 0000,003C,0180,F800,0000,0001

U 0402, 0000,003C,0180,F800,0000,0001

U 0403, 0000,003C,0180,F800,0000,0001

U 0404, 0818,001A,19E0,F8D8,0000,0061

U 0424, 0818,001A,19E0,F8D8,0000,0061

U 0405, 0000,003C,0180,F800,0000,0001

U 0406, 0818,001A,19E0,F8D8,0000,0061

U 0426, 0818,001A,19E0,F8D8,0000,0061

U 0407, 0000,003C,0180,F800,0000,0001

;14185 .TOC " I-stream decode forks : Address Specifier Evaluation"  
;14186 :  
;14187 : Control passes to this point by CALL.J/ASPC and returns to the call site "or"  
;14188 : 60, if the specifier is valid, or the call site "or" 61 if the specifier is  
;14189 : register mode, which will be invalid unless the specifier is a field source.  
;14190 : At the return, Q contains the longword that was in D at the entry. D and VA  
;14191 : contain the address implied by the specifier.  
;14192 :  
;14193 47E: ;-----;  
;14194 ASPC: Q\_IB.DATA, ;HANG HERE IF IB MUST STALL  
;14195 LAB\_R(SP1), ;GET SPECIFIER DATA FROM ISTREAM  
;14196 CLR\_IB.COND, ;LOAD LATCHES FROM BASE SPECIFIER  
;14197 PC PC+N, ;DISCARD BASE OPERAND SPECIFIER  
;14198 MCT/ALLOW\_IB.READ, ;STEP PC OVER IT  
;14199 SUB/SPEC.J/ASPC.B ;LET IB GET NEEDED DATA  
;14200 ;EVALUATE THE SPECIFIER  
;14201 400: ;-----;  
;14202 ASPC.B: J/R SVMOD ;S^# SHORT LITERAL NOT LEGAL AS ASRC  
;14203 ;  
;14204 401: ;-----;  
;14205 J/R SVMOD ;RESERVED MODE  
;14206 ;  
;14207 402: ;-----;  
;14208 J/R SVMOD ;QUAD/DOUBLE SHORT LITERAL  
;14209 ;  
;14210 403: ;-----;  
;14211 J/R SVMOD ;RESERVED MODE  
;14212 ;  
;14213 404: ;-----;  
;14214 Q\_D, ;REGISTER  
;14215 R7PRN\_LA+K[ZERO].RLOG, ;RECORD REGISTER NUMBER  
;14216 D\_ALU, ;GET REGISTER CONTENTS TO D  
;14217 RETURN61 ;RETURN IT IN CASE FIELD SOURCE  
;14218 ;  
;14219 424: ;-----;  
;14220 Q\_D, ;WRITE REGISTER  
;14221 R7PRN\_LA+K[ZERO].RLOG ;RECORD REGISTER NUMBER  
;14222 D\_ALU, ;GET REGISTER CONTENTS TO D  
;14223 RETURN61 ;RETURN IT IN CASE FIELD SOURCE  
;14224 ;  
;14225 405: ;-----;  
;14226 J/R SVMOD  
;14227 ;  
;14228 406: ;-----;  
;14229 Q\_D, ;QUAD REGISTER  
;14230 R7PRN\_LA+K[ZERO].RLOG, ;RECORD REGISTER NUMBER  
;14231 D\_ALU,RETURN61 ;RETURN CONTENTS TO CALLER  
;14232 ;  
;14233 426: ;-----;  
;14234 Q\_D, ;WRITE QUAD REGISTER  
;14235 R7PRN\_LA+K[ZERO].RLOG, ;RECORD REGISTER NUMBER  
;14236 D\_ALU,RETURN61 ;RETURN CONTENTS TO CALLER  
;14237 ;  
;14238 407: ;-----;  
;14239 J/R SVMOD ;ILLEGAL QUAD REG

ZZ-ESOAA-124.0 ; ASPC .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame M13 Sequence 374  
 ; F1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 ; ASPC .MIC [600,1204] I-stream decode forks : Address Specifier Evaluation

Page 373

M 13

:14240 ;ADDRESS SPECIFIER EVALUATION, CONTINUED  
 :14241  
 :14242 408: -----  
 :14243 ASPC.DR:Q\_D,D&VA\_LA, : (R)  
 :14244 LC RC[T?], :RECOVER INDEX, IF ANY  
 :14245 RETURN60 :RETURN IT  
 U 0408, 0800,003E,01E0,F938,0200,0060  
 :14246  
 :14247 409: -----  
 :14248 R (PRN)\_LA+K[SP1.CON].RLOG, :UPDATE THE STACK POINTER  
 :14249 J/ASPC.DR :THEN LOAD UN-INCREMENTED ADDR  
 :14250  
 :14251 40A: -----  
 :14252 Q\_D,R(PRN)\_LA-K[SP1.CON].RLOG, :-(R) AUTO DECREMENT  
 :14253 D\_ALU, : USE DECREMENTED ADDR  
 :14254 J7ASPC.DF :GO LOAD LC BEFORE RETURNING  
 U 040A, 0818,0004,15E0,F8D8,0000,09A6  
 :14255  
 :14256 40B: -----  
 :14257 Q\_D,VA\_LA :@ (R) + AUTO INCREMENT DEFERED  
 :14258  
 :14259  
 :14260 D[LONG] CACHE, :GET INDIRECT WORD  
 :14261 R(PRN)\_A+K[.4].RLOG, : WHILE UPDATING REGISTER  
 :14262 J/ASPC.DF :THEN JOIN COMMON CODE  
 :14263  
 :14264 40C: -----  
 :14265 RC[T?] LA.CTX, :INDEX MODE, CONTEXT SHIFT INDEX  
 :14266 CALL,J7ASPC :GO AROUND AGAIN  
 :14267  
 :14268 46C: -----  
 :14269 D&VA\_D+LC, :RETURN THE INDEXED VALUE  
 :14270 RETURN60  
 :14271  
 :14272 40D: -----  
 :14273 Q\_D,D&VA\_Q+LB.PC, :D(R) DISPLACEMENT MODE.  
 :14274 C[R.IB.SPEC, :DISCARD THE SPECIFIER  
 :14275 LC RC[T?], :LOAD UP INDEX, IF ANY  
 :14276 RETURN60  
 :14277  
 :14278 40F: -----  
 :14279 Q\_D,VA\_Q+LB.PC, :@D(R) DISPLACEMENT DEFERED  
 :14280 C[R.IB.SPEC :DROP THE SPECIFIER  
 :14281  
 :14282  
 :14283 D[LONG]\_CACHE :GET INDIRECT, GO USE IT AS ADDR  
 :14284  
 :14285  
 :14286 ASPC.DF:VA\_D, :USE POINTER AS ADDRESS  
 :14287 LC RC[T?] :RECOVER INDEX, IF ANY  
 :14288 RETURN50 :RETURN IT  
 U 046C, 0811,0016,0180,F800,0200,0060  
 U 040D, D805,2016,01E0,F938,0200,0060  
 U 040F, D005,2014,01E0,F800,0200,09A4  
 U 09A4, 0000,003C,0180,4000,0000,09A6  
 U 05A6, 0001,003E,0180,F938,0200,0060

ZZ-ESOAA-124.0 ; ASPC .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame N13 Sequence 375  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 374  
 : ASPC .MIC [600,1204] I-stream decode forks : Address Specifier Evaluation

N 13

:14289 ;HERE ARE VARIANTS OF THE ASPC ENTRY POINTS FOR R=PC

:14290

U 0414, 0000,003C,0180,F800,0000,0001 :14291 414: ;-----; ;PC REGISTER MODE

:14292 J/RSVMOD

:14293

U 0415, 0000,003C,0180,F800,0000,0001 :14294 415: ;-----; ;ILLEGAL REGISTER MODE, R=PC

:14295 J/RSVMOD

:14296

U 0416, 0000,003C,0180,F800,0000,0001 :14297 416: ;-----; ;PC QUAD REGISTER MODE

:14298 J/RSVMOD

:14299

U 0417, 0000,003C,0180,F800,0000,0001 :14300 417: ;-----; ;ILLEGAL QUAD REGISTER MODE, R=PC

:14301 J/RSVMOD

:14302

U 0418, 0000,003C,0180,F800,0000,0001 :14303 418: ;-----; ;(PC)

:14304 J/RSVMOD

:14305

U 0419, D814,0038,01E0,F800,0000,09A8 :14306 419: ;-----; ;(PC)+ IMMEDIATE MODE

:14307 Q\_D,

:14308 D\_P,

:14309 CLR.IB.SPEC ;GET PC WHICH THE IB INCREMENTED

:14310

U 09A8, 0819,0002,1580,F938,0200,0060 :14311

:14312 D&VA,D-K[SP1.CON]. ;COMPUTE THE UNINCREMENTED ADDRESS

:14313 LC\_R[C[T?]], ;RECOVER INDEX, IF ANY

:14314 RETURN60

U 041A, 0000,003C,0180,F800,0000,0001 :14315

:14316 41A: ;-----;

:14317 J/RSVMOD ;-(PC)

:14318

U 041B, DC01,203E,01E0,F938,0200,0060 :14319 41B: ;-----;

:14320 Q\_D,D&VA\_Q.

:14321 LC\_R[C[T?]], ;@PC)+ ABSOLUTE MODE

:14322 CLR.IB.SPEC, ;GET BACK INDEX

:14323 RETURN60

U 041C, 0000,003C,0180,F800,0000,00C1 :14324

:14325 41C: ;-----; ;INDEX MODE, R=PC

:14326 J/RSVMOD

:14327

U 041D, 0000,003C,0180,F800,0000,0001 :14328 41D: ;-----; ;NESTED INDEX MODE, R=PC

:14329 J/RSVMOD

B 14

```

;14330 ;HERE WHEN IB ROMS BELIEVE WE SHOULDN'T GET HERE
;14331
;14332 487: ;-----;
;14333     CALL,J/EH.US EQ ;'UNUSED' LOCATION IN IB ROM
;14334
;14335 ;HERE OFF ASPC, WHEN INSTRUCTION BUFFER DOES NOT HAVE ENOUGH DATA
;14336
;14337 47C: ;-----;
;14338     CALL,J/IB.TBM ;TB MISS. REFILL IT
;14339
;14340 47D: ;-----;
;14341     CALL,J/IB.ERR ;ANY ERROR. FIND OUT WHAT HAPPENED
;14342
;14343 47E: ;-----;
;14344     ; ASPC: ;STALL, WAITING FOR THE DATA
;14345
;14346 47F: ;-----;
;14347     J/INT.B ;INTERRUPT REQUEST DETECTED
;14348 ;BACKUP REGISTERS AND TAKE INTERRUPT
;14349 =(*
;14350 INT.B: ;-----;
;14351     RC[PC.SV].PC, ;SAVE PC WHERE BAKUP.PC WILL FIND IT
;14352     CALL,RLOG.EMPTY?,J/BAKUP.RGS ;GO RESTORE REGISTERS AND PC
;14353
;14354 INT.I: ;-----;
;14355     Q_ID[PSL], ;HERE ON INTERRUPT IN MIDST OF INSTR
;14356     ALU_-1,D_ALU.RIGHT2,SI/ZERO ;GET CURRENT PSL
;14357 A .PA.30:
;14358 ;-----;
;14359     D_D.AND.Q ;CLEAR TP (CM =0 ANYWAY)
;14360
;14361 ;-----;
;14362     ID[PSL] D, ;PUT BACK PSL
;14363     INTERRUPT.REQ?,J/INTIO
;14364
;14365 .LIST      ;Re-enable full listing
  
```

ZZ-ESOAA-124.0 ; ASPC .MIC [600,1204] I-stream decode for 14-Jan-82 Fiche 2 Frame C14 Sequence 377  
; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 376  
; ASPC .MIC [600,1204] I-stream decode forks : Address Specifier Evaluation

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14365: This page intentionally left blank.

ZZ-ESOAA-124.0 : FIELD .MIC [600,1204] FIELD.MIC 14-Jan-82 Fiche 2 Frame D14 Sequence 378  
: P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 377  
: FIELD .MIC [600,1204] FIELD.MIC

D 14  
14-Jan-82  
15:30:16  
VAX11/780 Microcode : PCS 01, FPLA OE, WCS124  
Fiche 2 Frame D14 Sequence 378  
Page 377  
:14366 .TOC 'FIELD.MIC'  
:14367 .TOC 'Revision 1.1'  
:14368 : P. R. Guilbault  
:14369 :

:14370 .NOBIN ..  
:14371 .TOC .. Revision History"  
:14372 ..  
:14373 : 01 Remove absolute jumps.  
:14374 : 00 Start of history  
:14375 ..

:14376 .BIN  
:14377 .NOLIST ;Disable listing of PCS code for quickie assemblies

ZZ-ESOAA-124.0 ; FIELD .MIC [600,1204] Field instructions 14-Jan-82 Fiche 2 Frame E14 Sequence 379  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 378  
 ; FIELD .MIC [600,1204] Field instructions : FFS, FFC, CMPV, CMPZV, EXTZV, EXTZV

U 034E, 0001,203C,C0B7,FAF8,0096,6054	:14378 .TOC " Field instructions : FFS, FFC, CMPV, CMPZV, EXTZV, EXTZV"
	:14379 ;HERE WITH SIZE OPERAND IN D, POSITION IN Q
	:14380 ;34E:
	:14381 FF:
	:14382 CMPV:
	:14383 EXTV: -----
	:14384 SC Q, :CALL SITE FOR INVOKING ASPC SUBR
	:14385 R[R15] Q, :MOVE POSITION (LOW BITS) TO SC
	:14386 Q Q.RIGHT,SI/ASHR, :SAVE POSITION IN R15 FOR FFX
	:14387 C[R.SDBSS, :GET POSITION/2
	:14388 EALU_K[.FFFF],CLK.UBCC :INIT SS FOR BRANCHES
	:14389 :SET EALU N=1, Z=0
	:14390 =10****0: -----
	:14391 Q Q.RIGHT2,SI/ASHR, :CALL SITE FOR VSRC SPECIFIER EVALUATION
	:14392 FE SC, :GET POSITION/8
	:14393 SC_D.0XT[BYTE]-K[.1], :MOVE LOW BITS OF POSITION TO FE
	:14394 CALL,J/EXTV.2 :GET SIZE -1 TO SC
	:14395 :GO CALCULATE BASE
	:14396 =11****0: -----
	:14397 Q_Q+D, :RETURN HERE WITH BASE ADDRESS IN D
	:14398 D_D.LEFT, :(POSITION/8)+BASE TO Q
	:14399 FE_SC-K[.1F], :BASE *2
	:14400 SC_FE, :GET S-32 IN FE
	:14401 SC?,J/EXTV.3 :LOW BITS OF POSITION TO SC
	:14402 :TEST SIZE .LEQU. 32
	:14403 =100 :-----
	:14404 Q_D, :RETURN HERE WITH REGISTER
	:14405 D_Q.RIGHT2, :SAVE LOW REGISTER IN Q A MOMENT
	:14406 FE_SC-K[.1F], :D IS POSITION/32
	:14407 SC_FE, :GET S-32 TO FE
	:14408 SC?,J/EXTV.3 :AND POSITION TO SC
	:14409 =100 :-----
	:14410 Q_D, :SC .EQL. 0 (SIZE =1)
	:14411 SC_SC+FE, :GET P+S-32
	:14412 =100 D_Q, :GET LOW REGISTER WITH FIELD
	:14413 Q_R(PRN+1), :GET HIGH REGISTER
	:14414 D_NE.0?,J/EXTV.5 :MAKE SURE POSITION WAS LESS THAN 32
	:14415 =100 :-----
	:14416 D_0,Q_0, :SC .LSS. 0 (SIZE =0)
	:14417 SC_FE, :FIELD OF SIZE 0 IS ZERO
	:14418 SUB/SPEC,J/EXTV.8 :GET SIZE -32 FOR FFX USE
	:14419 :FIND OUT WHAT TO USE IT FOR
	:14420 =100 :-----
	:14421 D_0,Q_0, :0 .LSS. SC .LSS. 32 (SIZE VALID)
	:14422 SC_SC+FE, :GET P+S-32
	:14423 D_Q, :GET LOW REGISTER WITH FIELD
	:14424 Q_R(PRN+1), :GET HIGH REGISTER
	:14425 D_NE.0?,J/EXTV.5 :MAKE SURE POSITION WAS LESS THAN 32
	:14426 =100 :-----
	:14427 D_0,Q_0, :SC .GEQ. 32
	:14428 J/RSVOPR
	:14429 =;END OF SC TEST

ZZ-ESOAA-124.0 ; FIELD .MIC [600,1204] Field instructions 14-Jan-82 Fiche 2 Frame F14 Sequence 380  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 379  
 ; FIELD .MIC [600,1204] Field instructions : FFS, FFC, CMPV, CMPZV, EXTV, EXTZV

;14432 :HERE TO GET BASE OF FIELD.  
 ;14433 : RETURN ABOVE, WITH POSITION/8 IN Q, BASE ADDRESS IN D  
 ;14434  
 ;14435  
 ;14436 EXTV.2: D\_Q, :POSITION /8 NOW IN D  
 ;14437 LAB\_R(SP1). :LOAD LATCHES WITH SPECIFIER REGISTER  
 ;14438 Q\_IB.DATA, :ASK IB FOR SPECIFIER DATA  
 ;14439 CCR\_IB.COND. :CLEAR IT  
 ;14440 PC\_PC+N, :STEP PC OVER IT  
 ;14441 SUB/SPEC,J/ASPC.B :GO EVALUATE BASE SPECIFIER ADDRESS  
 ;14442  
 ;14443 :HERE FOR FIELD INSTRUCTIONS WHEN THE FIELD IS  
 ;14444 : IN MEMORY, AS OPPOSED TO A REGISTER.  
 ;14445  
 ;14446 =100 :-----;SC .EQL. 0 (SIZE =1)  
 ;14447 EXTV.3: VA\_Q.ANDNOT.K[.3]. :LONGWORD ADDRESS OF FIELD  
 ;14448 D\_D.LEFT2, :BASE NOW \*8 IN D  
 ;14449 J7EXTV.4  
 ;14450  
 ;14451 :-----;SC .LSS. 0 (SIZE =0)  
 ;14452 D\_0,Q\_0. :ANY FIELD OF SIZE 0 IS ZERO  
 ;14453 SC\_FE, :GET SIZE -32 FOR FFX  
 ;14454 SUB/SPEC,J/EXTV.8 :GO FIND OUT WHAT TO DO WITH IT  
 ;14455  
 ;14456 :-----;1 .LEQ. SC .LEQ. 31 (SIZE .LEQ. 32)  
 ;14457 VA\_Q.ANDNOT.K[.3]. :LONGWORD ADDRESS OF FIELD  
 ;14458 D\_D.LEFT2, :BASE NOW \*8 IN D  
 ;14459 J7EXTV.4  
 ;14460  
 ;14461 :-----;SC .GTR. 31 (SIZE .GTR. 32)  
 ;14462 J/RSVOPR :TAKE RESERVED OPERAND FAULT  
 ;14463  
 ;14464 :END OF SC TEST  
 ;14465  
 ;14466  
 ;14467 EXTV.4: Q\_D+K[SC] : (BASE \*8) + POSITION  
 ;14468  
 ;14469  
 ;14470 :-----;SC\_Q.AND.K[.1F], :GET P (POSITION IN LONGWORD) TO SC  
 ;14471 D[ONG]\_CACHE :GET LONGWORD CONTAINING FIELD

ZZ-ESOAA-124.0 ; FIELD .MIC [600,1204]  
; P1W124.MCR 600,1204]

MICR02 1L(03)  
Field instructions

Field instructions 14-Jan-82

G 14

14-Jan-82 15:30:16

Fiche 2 Frame G14

Sequence 381

VAX11/780 Microcode : PCS 01, FPLA OE, WCS124

Page 380

; FIELD .MIC [600,1204]

Field instructions

: FFS, FFC, CMPV, CMPZV, EXTV, EXTZV

:14472 ;AT THIS POINT, WE HAVE CALCULATED P, THE POSITION OF THE FIELD  
:14473 ;WITHIN AN ALIGNED LONGWORD, AND HAVE GOTTEN THAT LONGWORD CONTAINING THE  
:14474 ;LOW-ORDER BIT OF THE FIELD INTO D. WE MUST DETERMINE WHETHER THE FIELD  
:14475 ;EXTENDS INTO A SECOND LONGWORD, AND SHIFT THE FIELD INTO PLACE.

:14476

:14477

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:14480

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:14504

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:14506

:14507

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:14511

:14512

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:14514

:14515

=;END OF EALU N+Z TEST

ZZ-ESOAA-124.0 ; FIELD .MIC [600,1204] Field instructions 14-Jan-82 Fiche 2 Frame H14 Sequence 382  
; P1W124.MCR 600,1204] MICRC2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS1\_34 Page 381  
; FIELD .MIC [600,1204] Field instructions : FFS, FFC, CMPV, CMPZV, EXTV, EXTZV

H 14  
;14516 ;AT THIS POINT, THE DESIRED FIELD HAS BEEN POSITIONED IN D, SO THAT ITS  
;14517 ;MOST SIGNIFICANT BIT IS IN D31, AND SC CONTAINS THE FIELD SIZE -32.  
;14518 ; Q D  
;14519 ;-----\*-----  
;14520 ; \* 0 \* < S > ! \*  
;14521 ;-----\*-----  
;14522 ; \* \*  
;14523 ;-----\*-----  
;14524

U 0482, 0000,0D3C,0180,F800,0000,048E 14525 482: -----;EXTV OR CMPV  
;14526 EXTV.8: D31?,J/EXTV.9 ;TEST SIGN OF FIELD  
;14527  
;14528 ;HERE WE EXTEND THE FIELD TO A LONGWORD, AND EVALUATE THE FINAL SPECIFIER  
;14529 ; IF THIS IS EXTV OR EXTZV, THE FINAL SPECIFIER WILL BE 'WRITE' TYPE,  
;14530 ; AND THE CODE AT B-FORK WILL TRANSFER TO IRD AFTER STORING THE RESULT.  
;14531 ; IF THIS IS CMPV OR CMPZV, THE FINAL SPECIFIER IS 'READ' TYPE,  
;14532 ; AND B-FORK WILL GO ON TO EXECUTION AT CMP.  
;14533  
;14534 48E: -----;D31=0. FIELD IS POSITIVE (OR ZERO-EXT)  
;14535 EXTV.9: D\_DAL.SC, ;SIGN- OR ZERO- EXTEND THE FIELD  
;14536 B.FORK ;GO EVALUATE THE FOURTH SPECIFIER  
;14537  
U 048E, FD00,003F,01F0,F847,0000,0200 14538 48F: -----;D31=1. FIELD IS NEGATIVE  
;14539 Q\_NOT.Q,J/EXTV.9 ;SIGN-EXTENSION REQUIRES ONES

U 048F, 0001,2028,01C0,F800,0000,048E

ZZ-ESOAA-124.0 ; FIELD .MIC [600,1204] Field instructions 14-Jan-82 I 14  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA UE, WCS124 Fiche 2 Frame I14 Sequence 383  
 ; FIELD .MIC [600,1204] Field instructions : FFS, FFC, CMPV, CMPZV, EXT, EXTZV Page 382

:14540 ;HERE FOR FFS. FFC WITH THE SELECTED FIELD LEFT-ALIGNED IN D, AND Q ZERO.  
 :14541 ; SC HAS S-32, FOR SHIFTING THE FIELD INTO D, RIGHT ALIGNED.  
 :14542 ; R15 CONTAINS THE ORIGINAL POSITION.  
 :14543 ; IF THIS IS FFC, WE FIRST COMPLEMENT D TO CONVERT "CLEAR" TO "SET"  
 :14544  
 U 0481, 0801,0028,0180,F800,0000,0480 :14545 481: -----  
 :14546 FFC.1: D\_NOT.D ;SEARCH FOR ZEROS  
 :14547  
 U 0480, 0D18,0038,7550,F800,00F4,8981 :14548 480: -----  
 :14549 FFS.1: D\_DAL.SC, ;RIGHT-ALIGN THE FIELD IN D  
 :14550 SC\_SC+K[.20], ;RECOVER FIELD SIZE  
 :14551 ALU\_K[.20],LONG,CCK/INST.DEP ;GUESS WE WILL FIND A BIT  
 :14552  
 :14553  
 U 0981, 001F,2D00,01C0,F800,0000,04E5 :14554 Q\_0-D, ;NEGATE D TO Q  
 :14555 D\_NE\_0? ;ARE ANY SET (FFS) OR CLEAR (FFC)?  
 :14556  
 U 04E5, 0001,C03C,0180,F800,0070,0984 :14557 =101 :-----  
 :14558 ALU\_D,SET.CC(INST), ;MAKE ALU ZERO, SET PSL<Z>  
 :14559 J/FFS.3 ;GO ADD SIZE TO OLD POSITION  
 :14560  
 :14561  
 U 04E7, 081D,0034,8D80,F800,0084,6984 :14562 D\_D.AND.Q, ;LEAVE ONLY LEAST SIGNIFICANT ONE SET  
 :14563 SC\_K[.1F] ;SETUP 31 FOR CALCULATING BIT POSITION  
 :14564  
 :14565  
 U 0984, 0000,003C,01C0,FA78,008C,A985 :14566 FFS.3: SC\_SC-SHF.VAL, ;SC GETS BIT POSITION OF FIRST ONE  
 :14567 ; (SHF.VAL =0 IF D=0)  
 :14568 Q\_R[R15] ;GET STARTING POSITION  
 :14569  
 :14570  
 U 0985, F819,2017,1DF0,F847,0000,0300 :14571 D\_Q+K[SC], ;GET POSITION TO RETURN  
 :14572 WRITE.DEST,J/WRD ;GIVE IT BACK

J 14

ZZ-ESOAA-124.0 ; FIELD .MIC [600,1204] Field instructions 14-Jan-82 Fiche 2 Frame J14 Sequence 384  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 383  
 ; FIELD .MIC [600,1204] Field instructions : INSV

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:14573 .TOC   "      Field instructions : INSV"
:14574
:14575 ;THE VALUE TO BE INSERTED IS IN Q, AND THE FIELD POSITION IS IN D
:14576 ;TEMPS USED BY THIS ROUTINE ARE:
:14577 ;    ID[T0] = SOURCE, THE VALUE TO BE INSERTED
:14578 ;    RC[T1] = POSITION/8
:14579 ;    RC[T2] = ADDRESS OF LONGWORD CONTAINING LOW BIT(S) OF FIELD
:14580 ;    RC[T3] = THE MEMORY LONGWORD ADDRESSES BY T2, MASKED DOWN
:14581 ;    TO ONLY THE BITS TO BE PRESERVED.
:14582 ;    RC[T4] = MASKS
:14583
:14584 348: -----
:14585 INSV: SC_D,
:14586 Q_D.RIGHT2,SI/ASHR, ;LOW BITS OF POSITION TO SC
:14587 D_C, ;POSITION/4 IN Q
:14588 CLR_SD&SS, ;PREPARE NEW VALUE FOR SAVING IN ID TO
:14589 CALL_J/INSV.1 ;INIT FLAGS FOR EASIER BRANCHING
:14590
:14591 368: -----
:14592 LC_RC[T1], ;RETURN HERE WITH BASE IN D IF MEMORY
:14593 Q_D.LEFT3, ;GET POSITION/8 READY
:14594 FE_SC-K[.1F], ;ALSO BASE *8
:14595 SC_FE, ;GET S-32 TO FE
:14596 SC?,J/INSV.4 ;LOW BITS OF POSITION TO SC AGAIN
:14597 ;VALIDATE SIZE OPERAND
:14598 369: -----
:14599 D_Q.RIGHT2,SI/ZERO,Q_0, ;RETURN HERE IF BASE SELECTS REGISTER
:14600 FE_SC-K[.1F], ;GET P/32 IN D
:14601 SC_FE, ;GET S-32 IN FE
:14602 SC? ;POSITION TO SC
:14603
:14604 =100 :----- ;TEST SIZE-1
:14605 Q_ID[T0], ;SC=0 (SIZE=1)
:14606 RC[T4] 0+MASK+1, ;GET DATA TO BE INSERTED
:14607 FE_SC+FE,CLK.UBCC, ;BEGIN MASK GENERATION
:14608 D_NE.0?,J/INSV.2 ;CALCULATE P+S-32
:14609 ;IS POSITION LEGAL?
:14610 :----- ;SC.LSS.0 (SIZE =0)
:14611 CLR_IB.OPC ;GO ON TO NEXT INSTR
:14612 PC_PC+1,J/IRD
:14613
:14614 :----- ;SC.GTR.0
:14615 Q_ID[T0], ;GET DATA TO BE INSERTED
:14616 RC[T4] 0+MASK+1, ;BEGIN MASK GENERATION
:14617 FE_SC+FE,CLK.UBCC, ;CALCULATE P+S-32
:14618 D_NE.0?,J/INSV.2 ;IS POSITION LEGAL?
:14619
:14620 :----- ;SC.GEQ.32
:14621 J/RSVOPR
  
```

U 0348, 0C81,003D,00C7,F80C,0082,010A

U 0368, 00A1,143C,8DC0,F908,0185,A684

U 0369, 0881,343C,8DF8,F800,0185,A674

U 0674, 0003,0D10,C1F0,2DA0,0110,84FC

U 0675, C000,003C,0180,F804,4000,0062

U 0676, 0003,0D10,C1F0,2DA0,0110,84FC

U 0677, 0000,003C,0180,F800,0000,0106

ZZ-ES0AA-124.0 ; FIELD .MIC [600,1204] ; P1W124.MCR 600,1204] ; FIELD .MIC [600,1204] K 14  
 Field instructions 14-Jan-82  
 MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 Fiche 2 Frame K14 Sequence 385  
 Page 384

;14622 ;HERE TO INSERT A FIELD INTO A REGISTER  
 ;14623  
 ;14624 =0\* -----;D.EQL.0 (POSITION .LSSU. 32)  
 ;14625 INSV.2: D\_Q, ;PREPARE TO ROTATE INSERT DATA  
 ;14626 EALU.N?,J/INSV.2A ;IS FIELD ALL IN ONE REGISTER?  
 ;14627  
 ;14628 -----;D.NEQ.0 (POSITION .GEQU. 32)  
 ;14629 J/RSVOPR  
 ;14630  
 ;14631 =0'1\* -----;EALU N=0 (P+S .GEQ.32)  
 ;14632 INSV.2A:D DAL.SC, ;ALIGN THE INSERTION  
 ;14633 SC\_FE, ;P+S-32  
 ;14634 Q [A.ANDNOT.RC[T4], ;SAVE NON-FIELD BITS OF REGISTER  
 ;14635 J7INSV,3  
 ;14636  
 ;14637 : \*\*\*\*\*  
 ;14638 : \* Patch no. 065, PCS 0196 trapped to WCS 1188 \*  
 ;14639 : \*\*\*\*\*  
 ;14640  
 ;14641 -----;EALU N=1 (P+S .LSS. 32)  
 ;14642 D\_DAL.SC, ;ALIGN THE INSERTION  
 ;14643 SC\_FE, ;GET P+S-32  
 ;14644 Q\_RC[T4] ;GET PARTIAL MASK  
 ;14645  
 ;14646 -----;PREPARE MASK OF FIELD  
 ;14647 Q\_Q-MASK-1  
 ;14648 -----;STRIP OFF ALL BUT INSERTION  
 ;14649 D\_D.AND.Q  
 ;14650  
 ;14651  
 ;14652 -----;CLEAR FIELD FROM REGISTER  
 ;14653 Q\_R(PRN).ANDNOT.Q  
 ;14654  
 ;14655  
 ;14656 R(PRN)\_D.OR.Q,  
 ;14657 CLR.IB.OPC  
 ;14658 PC\_PC+1,J/IRD ;COMBINE FIELD WITH REST OF REGISTER  
 ;GO TO NEXT INSTR

U 04FC, 0C00,123C,0180,F800,0000,0196

U 04FE, 0000,003C,0180,F800,0000,0106

U 0196, 0D10,0024,01C0,F920,0081,09C4

U C19E, 0D10,0038,01C0,F920,0081,0988

U 0988, 0001,2008,01C0,F800,0000,0989

U 0989, 081D,0034,0180,F800,0000,09BC

U 09BC, 001C,0024,01C0,F858,0000,09BE

U 09BE, C01D,0030,0180,F8DC,4000,0062

ZZ-ESOAA-124.0 ; FIELD .MIC [600,1204] ; P1W124.MCR 600,1204] ; FIELD .MIC [600,1204] MICRO2 1L(03) Field instructions : INSV

L 14

Field instructions 14-Jan-82

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Fiche 2 Frame L14

VAX11/780 Microcode

: PCS 01, FPLA OE, WCS124

Sequence 386 Page 385

;14659 ;HERE FOR REGISTER INSERTION WHEN P+S IS GREATER THAN 32  
;14660  
;14661  
;14662 INSV.3: D\_D.AND.LC ;LOW PART OF INSERT INTO DATA  
;14663  
;14664  
;14665 R(PRN) D.OR.Q, ;COMBINE OLD DATA WITH INSERT  
;14666 Q\_ID[T0] ;GET BACK REST OF INSERT  
;14667  
;14668  
;14669 Q\_0+MASK+1, ;MASK FOR HIGH PART OF INSERT  
;14670 D\_DAL.SC ;GET HIGH PART OF INSERT  
;14671  
;14672 FI.PA.65:  
;14673  
;14674 D\_D.ANDNOT.Q ;STRIP INSERT DATA  
;14675  
;14676  
;14677 Q\_R(PRN+1).AND.Q ;CLEAR INSERTION PART OF REGISTER  
;14678  
;14679  
;14680 R(PRN+1) D.OR.Q, ;COMBINE INTO HIGH REGISTER  
;14681 CLR.IB.OPC,PC\_PC+1, ;GO TO NEXT INSTR  
;14682 J/IRD

ZZ-ESOAA-124.0 ; FIELD .MIC [600,1204]  
; PTW124.MCR 600,1204]  
; FIELD .MIC [600,1204]

MICR02 1L(03) Field instructions : INSV

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VAX11/780 Microcode

: PCS 01, FPLA 0E, WCS124

Fiche 2 Frame M14

Sequence 387

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U 010A, 0841,203D,C080,3D88,0000,037E

:14683 ;HERE IN INSV TO GET THE SIZE AND BASE OPERANDS  
:14684  
:14685 =0\*\*1\* :-----;CALL SITE FOR SIZE SPECIFIER EVALUATION  
:14686 INSV.1: IDE[T0]\_D, ;SAVE NEW VALUE FOR FIELD  
:14687 RC[T1]\_Q.RIGHT.SI/ASHR, ;POSITION/8 NOW IN RC T1  
:14688 D\_Q.RIGHT, ;AND D  
:14689 CALL.J/SPEC ;GO GET SIZE  
:14690  
:14691 :-----;RETURN HERE WITH SIZE IN D  
:14692 FE\_SC, ;MOVE POSITION OUT OF THE WAY  
:14693 SC\_D.0XT[BYTE]-K[.1], ;GET SIZE-1 TO SC  
:14694 D\_Q, ;LEAVE POS/8 IN Q ON RETURN  
:14695 LAB\_R(SP1). ;PREPARE TO EVALUATE BASE SPECIFIER  
:14696 Q\_IB.DATA,  
:14697 C[R].IB.COND.  
:14698 PC\_PC+N,  
:14699 SUB/SPEC,J/ASPC.B ;CALCULATE BASE ADDRESS  
:14700  
:14701 ;HERE FOR INSV ON A MEMORY FIELD  
:14702  
:14703 =100 :-----;SC\_EQL\_0 (SIZE =1)  
:14704 INSV.4: SC\_Q+K[SC], ;(BASE\*8) + POS TO SC  
:14705 LC\_RC[T1], ;LOAD LATCH WITH POSITION/8  
:14706 J/INSV.5  
:14707  
:14708 :-----;SC\_LSS\_0 (SIZE =0)  
:14709 CLR\_IB.OPC, ;DO NOTHING  
:14710 PC\_PC+1,J/IRD  
:14711  
:14712 :-----;0\_LSS\_SC\_LSS\_32 (SIZE VALID)  
:14713 SC\_Q+K[SC], ;SC GETS (BASE\*8) + POS  
:14714 LC\_RC[T1], ;GET POSITION OFFSET INTO LATCH  
:14715 J/INSV.5  
:14716  
:14717 :-----;SC\_GEQ\_32 (SIZE .GTR. 32)  
:14718 J/RSVOPR  
:14719  
:14720 =;END OF SC TEST

U 0684, 0019,2014,1D80,F908,0082,09CD

U 0685, C000,003C,0180,F804,4000,0062

U 0686, 0019,2014,1D80,F908,0082,09CD

U 0687, 0000,003C,0180,F800,0000,0106

N 14

:14721 ;HERE ON INSV OF A MEMORY OPERAND, HAVING VERIFIED THE SIZE  
 :14722 ; AND CALCULATED P, THE POSITION WITHIN AN ALIGNED LONGWORD  
 :14723  
 :14724  
 :14725 U 09CD, 0811,0014,A180,F800,0084,49CE INSV.5: SC SC,ANDNOT.K[.FFE0], :SC IS NOW POSITION IN LONGWORD  
 :14726 D\_D+LC :D IS BYTE ADDRESS OF FIELD  
 :14727  
 :14728  
 :14729 U 09CE, 0019,0024,0D80,F990,0310,89D0 VA\_D,ANDNOT.K[.3]. :CALCULATE LONGWORD ADDRESS OF FIELD  
 :14730 RCT2] ALU, :SAVE IT FOR WRITING BACK  
 :14731 FE\_SC+FE, :P+S-32  
 :14732 CLR.UBCC :WATCH FOR P+S .GTR. 32  
 :14733  
 :14734  
 :14735 Q\_0+MASK+1: :ZEROS TO RIGHT OF FIELD  
 :14736 RCT4] ALU: :KEEP HANDY  
 :14737 SC\_FE: :GET P+S-? TO SC  
 :14738 FE\_SC-K[.20]: :P-32 TO FE  
 :14739 D[LONG]\_CACHE.WCHK: :GET FIELD  
 :14740 EALU.N? :DOES IT CROSS LONGWORD BOUNDARY?  
 :14741  
 :14742 ; \*\*\*\*\*  
 :14743 ; \* Patch no. 036, PCS 09D0 trapped to WCS 1170 \*  
 :14744 ; \*\*\*\*\*  
 :14745  
 :14746 =011\* :----- U 02F6, 001D,0024,C1F0,2D9B,0181,09D5 EALU N=0, FIELD LIES ACROSS BOUNDARY  
 :14747 RCLT3] D.ANDNOT.Q. :SAVE LOW PART OF MEMORY DATA  
 :14748 Q\_ID[T0]. :GET DATA TO BE INSERTED  
 :14749 SC\_FE. :GET P-32 FOR ALIGNING INSERT DATA  
 :14750 FE\_SC. :SAVE P+S-32 (WHICH IS POSITIVE)  
 :14751 VA\_VA+4. :ADDR OF SECOND LONGWORD  
 :14752 J/INSV.6  
 :14753  
 :14754 U 02FE, 0001,2008,C1F0,2DA0,0081,09D1 RCT4]\_Q-MASK-1. :EALU N=1, FIELD IS IN ONE LONGWORD  
 :14755 SC\_FE. :MASK FOR BITS OF MEMORY TO DISCARD  
 :14756 Q\_ID[T0] :GET P-32 FOR SHIFT  
 :14757 :GET DATA TO INSERT  
 :14758  
 :14759 =;END OF EALU N TEST  
 :14760  
 :14761 FI.PA.36:  
 :14762  
 :14763 U 09D1, 0D11,0024,01C0,F920,C000,09D4 Q\_D.ANDNOT.RCT4]. :CLEAR THE FIELD OF MEMORY WORD  
 :14764 D\_DAL.SC :ALIGN THE INSERT DATA  
 :14765  
 :14766 U 09D4, 0811,0034,0180,F800,0000,09E1 D\_D.AND.LC. :DROP JUNK NOT TO BE INSERTED  
 :14767 J7INSV.7 :GO COMBINE AND STORE  
 :14768

ZZ-ESOAA-124.0 ; FIELD .MIC [600,1204] Field instructions 14-Jan-82  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124  
 : FIELD .MIC [600,1204] Field instructions : INSV

B 15

Fiche 2 Frame B15

Sequence 389

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;14769 ;HERE WHEN THE FIELD LIES ACROSS A LONGWORD BOUNDARY  
 ;14770  
 ;14771  
 ;14772 INSV.6: D\_DAL.SC, ;ALIGN THE INSERT DATA BY POSITION  
 ;14773 FE\_SC+KE[.20], ;RESTORE P TO FE  
 ;14774 SC\_FE ;AND P+S-32 TO SC  
 ;14775  
 ;14776  
 ;14777 Q\_D.AND.RC[T4], ;GET DESIRED PART OF THE INSERT  
 ;14778 D[LONG]\_CACHE.WCHK ;AND THE OTHER MEMORY DATA  
 ;14779  
 ;14780  
 ;14781 VA\_RC[T2], ;RELOAD ADDR OF FIRST LONGWORD  
 ;14782 Q\_D, ;HOLD NEXT MEMORY DATA AT SIDE  
 ;14783 D\_Q ;GET THE INSERT FIELD INTO D  
 ;14784  
 ;14785  
 ;14786 D\_D.OR.RC[T3] ;COMBINE NEW INSERT WITH OLD MEMORY DATA  
 ;14787  
 ;14788  
 ;14789 CACHE\_D[LONG], ;WRITE BACK LOW PART OF FIELD  
 ;14790 RC[T4]\_0+MASK+1, ;GET MASK FOR MEM SECOND PART  
 ;14791 SC\_FE ;P TO SC  
 ;14792  
 ;14793  
 ;14794 D\_Q.AND.RC[T4], ;STRIP LOW BITS FROM SECOND PART  
 ;14795 VA\_VA+4, ;GET ADDR OF HIGH PART AGAIN  
 ;14796 Q\_ID[T0] ;GET INSERT DATA AGAIN  
 ;14797  
 ;14798  
 ;14799 Q\_D ;SAVE MEM PART2  
 ;14800 D\_DAL.SC ;ALIGN THE INSERT  
 ;14801  
 ;14802  
 ;14803 D\_D.ANDNOT.LC ;DISCARD JUNK FROM INSERT  
 ;14804  
 ;14805  
 ;14806 INSV.7: D\_D.OR.Q, ;COMBINE INSERT WITH MEMORY DATA  
 ;14807 J7STOR.L ;PUT IT BACK IN MEMORY  
 ;14808  
 ;14809 .LIST ;Re-enable full listing

ZZ-ESOAA-124.0 ; CHAR .MIL [600,1204] CHAR.MIC 14-Jan-82 14-Jan-82 15:30:16 C 15 Fiche 2 Frame (15 Sequence 390  
; P1W124.MCR 600,1204] MICRO2 1L(03) VAX11/780 Microcode : PCS 01, FPLA 0E, W(S124 Page 389  
; CHAR .MIC [600,1204] CHAR.MIC

:14810 .TOC "CHAR.MIC"  
:14811 .TOC "Revision 1.3"  
:14812 : P. R. Guilbault  
:14813

:14814 .NOBIN ..  
:14815 .TOC .. Revision History"

:14816  
:14817 : 01 Change macro names that deal with conditions codes.  
:14818 : Comment patch no. 095 MOVCS optimization.  
:14819 : 00 Create this file by merging MACCOM.MIC, MOV.MIC, SKP.MIC, SPAN.MIC, CMP.MIC, MATCH.MIC, and MTC.MIC  
:14820 : Start of history  
:14821

:14822 .BIN  
:14823 .NOLIST :Disable listing of PCS code for quickie assemblies

ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] Character string 14-Jan-82 Fiche 2 Frame D15 Sequence 391  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 390  
 ; CHAR .MIC [600,1204] Character string : Utilities

;14824 .TOC " Character string : Utilities"  
 ;14825  
 ;14826 :ALGORITHM:  
 ;14827 AS PART OF INITIALIZATION OF SOME STRING INSTRUCTIONS,  
 ;14828 CLEAR PSL CONDITION CODES  
 ;14829  
 ;14830 :INPUTS:  
 ;14831 CALLED WITH PSL IN Q  
 ;14832  
 ;14833 :OUTPUTS:  
 ;14834 ID/PSL WRITTEN WITH COND CODES ALL 0  
 ;14835  
 ;14836 :RETURN:  
 ;14837 ALWAYS RETURNS 40  
 ;14838  
 ;14839 ;-----;  
 CLRPSLCC:  
 ;14840 D\_Q.ANDNOT.K[.F], ;CLEAR PSL CC BITS  
 ;14841 Q\_D ;PRESERVE D AS PASSED IN Q  
 ;14842 FE\_K[.F] ;FE IS USED AS FLAG FOR FPD  
 ;14843 ;FE NOT 0 = EXCEPTION,  
 ;14844 ;FE = 0 = INTERRUPT  
 ;14845 ;-----;  
 ;14846 ID[PSL]\_D, ;PSL CC ALL CLEAR  
 ;14847 D\_Q, ;RESTORE D  
 ;14848 RETURN40 ;  
 ;14849  
 ;14850 :ALGORITHM:  
 ;14851 WHEN AN INTERRUPT OR EXCEPTION HAS BEEN NOTED BY A STRING INSTRUCTION,  
 ;14852 THIS ROUTINE SAVES SOME VULNERABLE DATA IN R0<31:16> BEFORE  
 ;14853 HANDLING THE INT/EXC SO THE INSTRUCTION CAN BE RESUMED.  
 ;14854 JUMPS TO FPD.RTN IF AN EXCEPTION OR INTIO IF AN INTERRUPT PENDING.  
 ;14855  
 ;14856 :INPUTS:  
 ;14857 STATE=8 BITS OF DATA TO BE SAVED(CONTENTS VARY WITH EACH INSTR)  
 ;14858  
 ;14859 :OUTPUTS:  
 ;14860 R0<31:24>=PC DELTA, <23:16>=STATE, <15:00>=R0 AS PASSED  
 ;14861  
 ;14862 =00 ;-----;  
 FPDPACK:  
 ;14863 SC\_STATE, ;PREPARE TO SAVE STATE REG  
 ;14864 CALL,J/BAKUP.PC, ;BAKUP WILL RETURN PC DELTA  
 ;14865 Q\_PC ;IF GIVEN THE CURRENT PC IN Q  
 ;14866  
 ;14867 =10 ;-----;  
 ;14868 D\_D.SWAP, ;PC DELTA RETURNED IN D<7:0>  
 ;14869 ;PUT IT IN D<31:24>  
 ;14870 ;STATE TO Q  
 ;14871  
 ;14872 = Q\_SC ;  
 ;14873  
 ;14874 ;-----;  
 ;14875 SC\_K[.FFF8] ;SC\_-8 FOR RIGHT SHIFT 8

U 09E4, 0819,2024,61E0,F800,0104,69E5  
 U 09E5, 0C00,003E,3D80,3C00,0000,0040  
 U 06D8, 0014,0039,01C0,F800,1480,0EB8  
 U 06DA, 0B18,0038,1DC0,F800,0000,09E6  
 U 09E6, 0000,003C,7180,F800,0084,69E8

ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] Character string 14-Jan-82 E 15 Fiche 2 Frame E15 Sequence 392  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 391  
 ; CHAR .MIC [600,1204] Character string : Utilities

U 09E8, 0D18,0034,C1C0,FA00,0081,09E9  
 U 09E9, 001D,0C30,0180,FA80,0000,04F3  
 U 04F3, 0000,0E3C,0180,F800,0000,0F8D  
 U 04F7, 0000,003C,0180,F800,0000,0EBB  
 U 09EC, 0018,0038,1980,FA98,0000,09ED  
 U 09ED, 0018,0038,1980,FA80,0000,09EE  
 U 09EE, 0018,0038,1980,FAA8,0000,09F0  
 U 09F0, 0018,0038,1980,FAA0,0000,09F1  
 U 09F1, 0018,1238,1980,FA90,2000,05AE

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;14876 FPDPACK1:  

;14877  

;14878 D_DAL,SC, ;STATE TO Q<31:24>  

;14879 ;PC DELTA TO D<23:16>  

;14880 SC_FE ;MOVE INT/EXC FLAG TO SC TO TEST IT  

;14881 Q_R[R0].AND.K[.FFFF] ;PRESERVE LOW WORD OF R0  

;14882  

;14883  

;14884 =011 R[R0]_D.OR.Q.BEN/MUL ;R0=STATE,PC DELTA, R0<15:0>  

;14885 ;SC EQ 0?  

;14886 BEN/INTERRUPT,J/INTIO ;SC NE 0. INTIO RTN WILL DECIDE  

;14887  

;14888 : *****  

;14889 : * Patch no. 030, PCS 04F3 trapped to WCS 1162 *  

;14890 : *****  

;14891 ;111----- ;IF INTERNAL OR EXTERNAL INTERRUPT  

;14892 J/FPD,RTN ;SC = 0. IT'S AN EXCEPTION  

;14893  

;14894  

;14895  

;14896  

;14897 :ALGORITHM:  

;14898 : THIS IS A SEQUENCE OF INSTRUCTIONS THAT MERELY ZERO  

;14899 : REGISTERS AS REQUIRED BY THE SRM FOR TERMINATING ASSORTED  

;14900 : INSTRUCTIONS. THIS SEQUENCE CAN BE ENTERED AT ANY POINT  

;14901 : DEPENDING ON THE INDIVIDUAL INSTRUCTION'S REQUIREMENTS.  

;14902  

;14903 :INPUTS:  

;14904 : NONE  

;14905  

;14906 :OUTPUTS:  

;14907 : SPECIFIED REGISTERS ARE ZEROED  

;14908 : JUMPS TO IB.FILL WITH PSL<FPD> CLEARED  

;14909  

;14910  

;14911 R24503ZERO:  

;14912 R[R3]_K[ZERO] ;R3_0  

;14913  

;14914  

;14915 R0245ZERO:  

;14916 R[R0]_K[ZERO] ;R0_0  

;14917  

;14918  

;14919 R245ZERO:  

;14920 R[R5]_K[ZERO] ;R5_0  

;14921  

;14922  

;14923 R24ZERO:  

;14924 R[R4]_K[ZERO] ;R4_0  

;14925  

;14926  

;14927 R2ZERO: R[R2]_K[ZERO], ;R2_0  

;14928 CLR.FPD, ;CLEAR FPD BIT  

;14929 BEN/EALU ;BRANCH ON REG WRITE FLAG
  
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ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] .MIC [600,1204] Character string 14-Jan-82 F 15  
; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Fiche 2 Frame F15 Sequence 393  
; CHAR .MIC [600,1204] Character string : Utilities VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 392

U 05AE, 2014,0038,0180,F801,4200,00AB :14930 =1110  
;14931 STRINGFINAL:  
;14932 ;-----;SIGN SRC  
;14933 PC&VA\_PC,FLUSH.IB,J/IB.FILL ;ALL DONE. BACK TO IB  
;14934  
;14935 :1111-----;  
;14936 R(SC) D,SET(CC(LONG), ;WRITE CRC RESULT IN REG  
;14937 J/STRINGFINAL ;  
;14938 ;-----;  
;14939  
;14940  
;14941 :ALGORITHM:  
;14942 SHIFTS D + Q SO THAT PC CAN BE RESET FROM PC DELTA SAVED ACROSS INT/EXC.  
;14943 ALSO GETS STATE REG CONTENTS READY TO BE RESTORED/USED.  
;14944 ; CLEARS R0<31:16>  
;14945  
;14946 :INPUTS:  
;14947 D+Q = SAVED R0, SC=-16  
;14948  
;14949 :OUTPUTS:  
;14950 PC RESET, R0<31:16>=0, R0<15:0>UNMOLESTED.  
;14951 D<7:0> = STATE, ASSUMING SET BY FPDPACK,  
;14952 OTHERWISE WHATEVER WAS IN R0<31:24>  
;14953  
;14954 :RETURN:  
;14955 ALWAYS RETURNS 100  
;14956  
;14957 ;-----;  
;14958 :FPDUNPACK:  
;14959 D\_DAL.SC, ;D<7:0>=PC DELTA,<15:8>=STATE  
;14960 R[R0]\_Q.AND.K[.FFFF] ;RESTORE R0  
;14961  
;14962 ;-----;  
;14963 Q\_D.AND.K[.FF], ;EXTRACT PC DELTA  
;14964 FE\_K[.FF], ;RESET FE SO LOOKS LIKE EXCEPTION  
;14965 D\_Q ;D\_R0 AS SAVED AT FPD TIME  
;14966  
;14967 ;-----;  
;14968 D\_D.SWAP, ;D<7:0>=STATE  
;14969 PC\_Q+PC,RETURN100 ;RESET PC  
;14970 ;-----;

U 09F2, 0D19,2034,C180,FA80,0000,09F4  
U 09F4, 0C19,0034,49C0,F800,0104,69F5  
U 09F5, 0815,2016,0180,F801,0200,0100

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:14971 .TOC   "      Character string      : MOVC3, MOVC5"
:14972
:14973 :GENERAL OVERVIEW OF MOVC3 + MOVC5
:14974
:14975 : REGISTER USAGE:
:14976 :R0 LENGTH OF STRING TO MOVE (BYTE-REVERSED, IN <31:16>)
:14977 :STATE AND PC-DELTA (IN FLTG PT FORMAT IN <15:0>)
:14978 :R1 ADDR OF SOURCE
:14979 :R2 LENGTH OF FILL (-1) IN <15:0>; SIGN IS IN STATE<6>
:14980 :IF POSITIVE, IMPLIES THERE'S FILL TO DO
:14981 :IF NEGATIVE, IT'S COMPLEMENT OF EXCESS SRC,
:14982 :I.E. DEST LENGTH - SRC LENGTH (-1) ; HENCE, NO FILL
:14983 :R3 DEST ADDR
:14984 :R5 ORIGINAL R0 DURING SRC MOVE.
:14985 :4 BYTES OF FILL CHAR DURING FILL MOVE.
:14986 :STATE:
:14987 :<1:0> 00 = LWD MOVE
:14988 :        01 = BYTE MOVE
:14989 :        10 = WORD MOVE
:14990 :        4 BACKWARDS(SRC MOVE IS IN BACKWARDS DIRECTION)
:14991 :        5 FILLING(VALID ONLY WHILE MOVING FILL)
:14992 :        6 NEED TO FILL(VALID ONLY WHILE MOVING SRC)
:14993 :        7 0 FOR MOVC3/5, 1 FOR MOVTC/TUC IN THOSE PLACES
:14994 :WHERE THE TWO OPERATIONS SHARE CODE
:14995 :INITIALLY, IF SRC ADDR > DEST ADDR, THERE'S A POSSIBILITY OF OVERWRITING
:14996 :SRC BEFORE IT'S MOVED, SO R1 + R3 ADJUSTED FOR BACKWARDS MOVE
:14997 :NAMELY, R1_R1+R0, R3_R3+R0, R5_R0
:14998 :AFTER SRC IS MOVED FROM HIGHEST ADDR TO LOWEST, R1_R1+R5, R3_R3+R5 AND
:14999 :CODE JOINS FORWARD EXECUTION.
:15000 :AFTER SRC MOVE, IF R2 >= 0, R0_R2 + DONE
:15001 :IF R2 < 0, THERE'S FILL TO CONSIDER. R2_0, R5_LWD OF FILL CHAR, SC NOT 0.
:15002 :R0_0-R2 (FILL COUNTER AS A POSITIVE NUMBER) + USES MAIN FORWARD CODE.
:15003 :WHICH BRINGS US TO FPD HANDLING:
:15004 :IN MAIN LOOP, SRC ADDR IN LB, DEST ADDR IN LA
:15005 :FOR COUNT, VARIES WITH OPERATION
:15006 :IN PARTICULAR, READ FAULT & WRITE FAULT - RC[T2].
:15007 :INTERRUPT - Q

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ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] Character string 14-Jan-82 Fiche 2 Frame H15 Sequence 395  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 394  
 : CHAR .MIC [600,1204] Character string : MOVC3/5 INITIALIZATION

H 15

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:15008 .TOC   "      Character string      : MOVC3/5 INITIALIZATION"
:15009
:15010
:15011 44A: ;-----
:15012 MOVC3: RC[T0] Q.OXT[WORD].      ;1ST ARG IS LENGTH
:15013 CALL,J7ASPC                  ;GET DEST ADDR
:15014
:15015
:15016 46A: R[R3]_D                  ;SAVE DEST ADDR
:15017
:15018
:15019 LC_RC[T0]&R1_ALU,ALU_Q       ;GET LENGTH + SAVE SRC ADDR
:15020
:15021
:15022 R[R2]_NOT.0,                 ;INITIALIZATION ONLY
:15023 STATE_K[ZERO]
:15024
:15025
:15026 ALU_0-K[ZERO], SET.CC(LONG). ;CHANGING C.C. ROM SAVES A CYCLE HERE
:15027 J/MOVIC
:15028
:15029
:15030 44E: ;-----
:15031 MOVC5: RC[T0] Q.OXT[WORD].      ;SAVE SRC LENGTH
:15032 CALL,J7SPEC                  ;GET FILL BYTE
:15033
:15034
:15035 R[C1]_Q,                      ;SAVE SRC ADDR
:15036 Q_D,                          ;COPY FILL BYTE
:15037 D-D.SWAP,                     ;D<31:24> = FILL CHAR
:15038 SC_K[F.FFF8],                ;PREPARE FOR A DAL
:15039 CALL, J/MOVCCMPC5            ;COLLECT DESTINATION LEN,ADDR
:15040
:15041
:15042 0C5E: ;RETURN FROM MOVCCMPC5 HERE WITH RC[T2] AND Q =DEST LEN.
:15043 MOVC5SETUP: ;R2<31:16>=2 FILL CHARS. RC[T1]=SRC ADDR, D=DEST ADDR,
:15044 ;RC[T0] = SRC LEN
:15045 ;**NOTE** - MOVTC & MOVTUC ENTER MOVC FLOWS HERE **
:15046
:15047 R[R3]_D,                      ;SAVE DEST ADDR
:15048 D_Q,                          ;GET DEST LENGTH
:15049
:15050
:15051 Q_RC[T1]                      ;SRC ADDR
:15052
:15053
:15054 LC_RC[T0]&R1_Q               ;SAVE SRC ADDR IN R1, LATCH SRC LENGTH
  
```

ZZ-ESOAA-124.0 : CHAR .MIC [600,1204] .MIC [600,1204] Character string 14-Jan-82 I 15 Fiche 2 Frame I15 Sequence 396  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 395  
 ; CHAR .MIC [600,1204] Character string : MOVC3/5 INITIALIZATION

	:15055	-----;	
	:15056	R[R2] D-LC-1, DT/WORD.	;DEST LENGTH - SRC LENGTH - 1
	:15057	SET.CC(WORD).	;SET CC'S ON WORD SUBTRACT A LA COMPARE
	:15058	STATE_K[.40]	;INITIALIZE STATE TO 'NEED TO FILL'
	:15059	-----;	
	:15060	-----;	
	:15061	D_R[R3].	;LOAD DEST ADDR INTO D FOR COMPARE.
	:15062	BEN/ROR	;TEST IF DEST LEN > SRC LEN
	:15063	-----;	
	:15064	=101 -----;PSL <C>	
	:15065	[LC_RC[T2], STATE_K[ZERO]	;DEST<=SRC, NO FILLS, MIN = DESTLEN
	:15066	-----;	
	:15067	:MOVC3 + MOVC5 CONVERGING POINT	
	:15068	:DEST ADDR IN D, SRC ADDR IN Q, MIN(SRCLEN,DESTLEN) IN LC	
	:15069	-----;	
	:15070	-----;	
	:15071	MOV C: Q D-Q,	;DEST ADDR-SRC ADDR
	:15072	C[K.UBCC,	;SEE IF FORWARDS OR BACKWARDS MOVE
	:15073	SC FE.	
	:15074	IRT?	;TEST IF MOVC OR MOVTC/TUC
	:15075	=10 -----;	;IR<1>. BREAKOUT MOVC3/MOVC5
	:15076	-----;	FROM MOVTC/MOVTC/TUC USING IR1
	:15077	D_K[.1F00].RIGHT.	;FAULT VECTORS FOR MOVC ARE F81,F82
	:15078	LAB_R[R1].	
	:15079	SET.FPD.	
	:15080	SC SC-FE.	;THIS IS AN INTERRUPTABLE INSTRUCTION
	:15081	C3T?. J/MOVCSSETFPD	;CLEAR SC
	:15082	-----;	
	:15083	;1*-----;	
	:15084	LAB_R[R1], D_K[.1F00].RIGHT.	;GET MOVC FAULT VECTOR IN D.
	:15085	Q 0. SS 0&SD 0. SET.FPD.	;INIT FAULT FLAG & SET FPD.
	:15086	IR0.C31?. J/MOVTCWHATDIR	;BREAK OUT ON OP AND DIRECTION

ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] .MIC [600,1204] Character string 14-Jan-82 J 15 Fiche 2 Frame J15 Sequence 397  
 : P1WT24.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 396  
 : CHAR .MIC [600,1204] Character string : MOVC3/5 INITIALIZATION

U 059C, 0010.0038,B5C7,3C00,0010,0686	:15087	=0*	;-----;ALU <C>
	:15088	MOVCSSETFPD:	
	:15089	ID[FPDA]_D, SS_08SD_0,	;SD TELLS FAULTS FROM INTERRUPTS
	:15090	Q LC,	;SRC ADDR > DEST ADDR.
	:15091	[CK.UBCC,	
	:15092	J/MOVCFPLP	;MOVE FORWARD
	:15093		
	:15094	;1*	
	:15095	ID[FPDA]_D, SS_08SD_0,	;MAY BE BACKWARDS MOVE; IF SRC OUT
	:15096	ALU Q-LC,	;OF RANGE OF DEST, CAN MOVE FORWARD
:15097	LA RA[3],		
:15098	CLR.UBCC,	;LATCH DEST ADDR	
:15099	J/MOVCBCKWD\$MAYBE		
:15100			
:15101			
:15102	:-----;		
:15103	SUBROUTINE TO BUMP R1 & R3 BY AMOUNT IN Q AND SET BACKWARDS FLAG.		
:15104	ALSO SETS SC=R3<1:0>. IF CALLED WITH BEN/C31 WITH C31 SET, DOES		
:15105	NOT RETURN BUT ENTERS FORWARD MOVE FLOWS.		
:15106	=0*	;-----;ALU <C>	
:15107	MOVCRBUMP:		
:15108	R[R3] LA+Q,	;ADJUST DEST ADDR	
:15109	SC ALU,	;TO BE USED FOR OFFSET INDICATOR	
:15110	STATE STATE.OR.K[.10],	;SET BACKWARDS BIT	
:15111	J/MOVCRBUMP.1		
:15112			
:15113	;1*		
:15114	D R[R3],	;IT'LL BE FORWARD DIRECTION	
:15115	Z?	;ANY TO DO	
:15116	J/MOVCFST		
:15117			
:15118			
:15119	-----;		
:15120	MOVCRBUMP.1:		
:15121	R[R1]_Q+LB,	;ADJUST SRC ADDR	
:15122	SC SC.ANDNOT.K[.FFF:],	;SAVE <1:0> OF DEST ADDR	
	RETURN2		

U 059E, 0011.2000,B587,3C98,0010,0770

U 05C4, 001C,0014,6580,FA98,1486,2A00

U 05C6, 0800,013C,0180,FA18,0000,06C6

U 0A00, 000D,2016,F180,FA88,0084,4002

ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] Character string 14-Jan-82 K 15 Fiche 2 Frame K15 Sequence 398  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 397  
 : CHAR .MIC [600,1204] Character string : MOVC3/5 INITIALIZATION

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:15123 : SUBROUTINE TO GET A LENGTH/ADDRESS PAIR OF SPECIFIERS
:15124 : USED BY MOVC, CMPC, MOVTC, MOVTUC.
:15125 :
:15126 :-----
:15127 =010**1* ;HANDLE CALL,SPEC + CALL,ASPC SEQ
:15128 MOVCCMPC5:
:15129     D,DAL,SC, :D<31:16> = 2BYTES OF FILL
:15130     A[U_0+K[.1]. :CLEAR OUT ALU CC
:15131     CLK,UBCC, :HANDY FOR LOOSER BEN/IR LATER
:15132     CALL,J/SPEC :WILL RETURN WITH D IN Q
:15133 :
:15134 :-----
:15135 =011**1* ;SPEC RETURNS 10
:15136     RCT2]_D.OXT[WORD], :SAVE DEST LENGTH
:15137     D,Q, :RESTORE 2 BYTES OF FILL CHAR
:15138     CALL,J/ASPC :THIS'LL PUT FILL BYTES BACK INTO Q
:15139 :
:15140 :-----
:15141 =111**1* ;SAVE 2 BYTES OF FILL IN R2<31:16>
:15142     R[R2]_Q.ANDNOT.K[.FFFF]
:15143 :
:15144 :-----
:15145     Q,RC[T2], :LOAD Q WITH (USUALLY) DEST LEN,
:15146     RETURN[800] :RETURN TO CALLER
  
```

U 00A2, 0D1B,0015,0580,F800,0010,037E  
 U 00B2, 0C03,403D,0180,F990,0000,047E  
 U 00F2, 0019,2024,C180,FA90,0000,0A01  
 U 0A01, 0010,003A,01C0,F910,0000,0800

ZZ-ES0AA-124.0 : CHAR .MIC [600,1204] .MIC [600,1204] Character string 14-Jan-82 L 15 Fiche 2 Frame L15 Sequence 399  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 398  
 ; CHAR .MIC [600,1204] Character string : MOVC3/5 MAIN LOOPS

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;15147 .TOC   "      Character string      : MOVC3/5 MAIN LOOPS"
;15148
;15149 ;COUNT IN Q. SAVE IN RC[T2] ON EVERY ITERATION
;15150 ;ALU CC <Z> SET ON Q
;15151 ;SC = 0 = NOT FILL
;15152 ;R5 = 4 BYTES OF FILL CHAR
;15153
;15154 =110 ;-----;INTERRUPT
;15155 MOVCFLP:
;15156     D_R[R3],          ;DEST ADDR
;15157     Z?                ;MORE TO DO?
;15158     J/MOVCFST
;15159
;15160 ;111-----;
;15161 MOVCINTF:
;15162     D_Q,              ;GET LOOP COUNTER IN D FOR SWAP,
;15163     J/MOVCPACKST       ;GO PACK STUFF INTO R0
;15164
;15165 ;NEXT 2 STATES PROVIDE FOR A TIMELY SAVING OF 1 STATE IF PLACED AT
;15166 ;THIS LOCATION
;15167
;15168 =100 ;-----;
;15169 MOVCREADJUST:           ;AFTER A BACKWARDS MOVE
;15170     LAB_R[R1]          ;SRC ADDR TO LB
;15171
;15172 ;101-----;
;15173     LA_RA[3],          ;DEST ADDR TO LA
;15174     CALL,J/MOVCRBUMP    ;WILL RETURN TO 111 OF CONSTRAINT
;15175
;15176 ;110-----;PART OF A Z? ALSO
;15177 MOVCFTST:
;15178     D_Q-K[.3]-1, RC[T2]_ALU, ;ASSUME 4 BYTES LEFT, SAVE NEW CT
;15179     C[K].UBCC,           ;SET C31 IF 4 OR MORE BYTES LEFT
;15180     STATE_STATE.ANDNOT.K[.3]. ;ASSUME LONGWORD TRANSFER
;15181     BEN/MUL,             ;BRANCH ON DEST OFFSET + IF FILL
;15182     J/MOVCOFFSET
;15183
;15184 ;111-----;END OF MOVC FORWARD(DUE TO BEN) OR
;15185 ;FROM CALL AT MOVCREADJUST
;15186 ;D NOT.R[R2], Q NOT.R[R2], ;GET -(FILL COUNT) IN D AND Q LOW
;15187 ;STATE STATE.ANDNOT.K[.30], ;CLEAR FILL + BACKWARDS BITS
;15188     BEN/STATE7-4,         ;NEED TO FILL?
;15189     J/MOVCMAYBEFILL
  
```

U 06B6, 0800,013C,0180,FA18,0000,06C6

U 06B7, 0000,003C,0180,F800,0000,0733

U 06C4, 0000,003C,0180,FA08,0000,06C5

U 06C5, 0000,003D,0180,F898,0000,05C4

U 06C6, 0819,2C08,0D80,F990,1414,46E0

U 06C7, 0800,1628,79C0 F890,1404,47A3

ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] Character string 14-Jan-82 Fiche 2 Frame M15 Sequence 400  
; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
; CHAR .MIC [600,1204] Character string : MOVC3/5 MAIN LOOPS

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;15190 =000 ;-----;BEN/MUL - ALL 8 WAYS
;15191 MOVCOFFSET:
;15192 LAB_R[R1], ;DEST ADDR = BYTE 0, NOT FILL
;15193 VA[A, ;LOAD SRC ADDR
;15194 ID[T2]_D, ;SAVE UPDATE COUNT
;15195 C3?; IS THERE ROOM FOR THIS LWD?
;15196 J/MOVCFWC

;15197
;15198 ;001-----;DEST ADDR = BYTE 1, NOT FILL
;15199 LAB_R[R1], ;DEST ADDR = BYTE 1, NOT FILL
;15200 VA[A, ;LOAD SRC ADDR
;15201 J/MOVCFB ;DEST ADDR = BYTE 2, NOT FILL
;15202 ;010-----;DEST ADDR = BYTE 2, NOT FILL
;15203 LAB_R[R1], ;DEST ADDR = BYTE 2, NOT FILL
;15204 VA[A, ;LOAD SRC ADDR
;15205 C3T?; IS THERE ROOM FOR THIS LWD?
;15206 J/MOVCFWD ;DEST ADDR = BYTE 3, NOT FILL
;15207 ;011-----;DEST ADDR = BYTE 3, NOT FILL
;15208 LAB_R[R1], ;DEST ADDR = BYTE 3, NOT FILL
;15209 VA[A, ;LOAD SRC ADDR
;15210 J/MOVCFB ;DEST ADDR = BYTE 0, FILL
;15211 VA[A, ;NECESSARY FOR FPD INTERFACE
;15212 J/MOVCFB ;COPY DECREMENTED COUNTER
;15213
;15214 ;100-----;DEST ADDR = BYTE 0, FILL
;15215 LAB_R[R1], ;NECESSARY FOR FPD INTERFACE
;15216 Q D, ;ROOM FOR 1 BYTE?
;15217 C3?; WILL THAT FIT?
;15218 J/MOVCFILLMORE

;15219
;15220 : ***** * Patch no. 095, PCS 06E4 trapped to WCS 119E *
;15221 : ***** * Patch no. 095, PCS 06E4 trapped to WCS 119E *
;15222 : ***** * Patch no. 095, PCS 06E4 trapped to WCS 119E *
;15223
;15224 ;101-----;DEST ADDR = BYTE 1, FILL
;15225 LAB_R[R1], ;NECESSARY FOR FPD INTERFACE
;15226 Q Q-K[.1], ;ROOM FOR 1 BYTE?
;15227 C[K.UBCC, ;STATE STATE.OR.K[.1],
;15228 STATE STATE.OR.K[.1], ;J/MOVCFILLWR
;15229
;15230
;15231 ;110-----;DEST ADDR = BYTE 2, FILL
;15232 LAB_R[R1], ;NECESSARY FOR FPD INTERFACE
;15233 Q D+K[.2], ;UPDATE COUNTER FOR A WORD MOVE
;15234 C[K.UBCC, ;WILL THAT FIT?
;15235 STATE STATE.OR.K[.2], ;C3?; IS THERE ROOM FOR THIS LWD?
;15236 C3?; IS THERE ROOM FOR THIS LWD?
;15237 J/MOVCFILLMORE ;DEST ADDR = BYTE 3, FILL
;15238
;15239 ;111-----;DEST ADDR = BYTE 3, FILL
;15240 LAB_R[R1], ;NECESSARY FOR FPD INTERFACE
;15241 Q Q-K[.1], ;C[K.UBCC, ;STATE STATE.OR.K[.1],
;15242 C[K.UBCC, ;J/MOVCFILLWR
;15243 STATE STATE.OR.K[.1], ;C3?; IS THERE ROOM FOR THIS LWD?
;15244

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ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] Character string N 15  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 14-Jan-82 15:30:16 Fiche 2 Frame N15 Sequence 401  
 ; CHAR .MIC [600,1204] Character string : MOVC3/5 MAIN LOOPS VAX11/780 Microcode : PCS 01, FPLA OE, WCS124 Page 400

```

:15245 =0* ;-----;ALU <C>
:15246 MOVCFWC:
:15247 D_Q-K[.2], ;NOT ENOUGH ROOM FOR A LWD
:15248 C[K].UBCC,
:15249 D(1)?,
:15250 J/MOVCFB ;ROOM FOR 1 BYTE OR 1 WORD?
:15251
:15252 ;1*-----
:15253 MOVCFCL:
:15254 D[LONG]_CACHE, ;DECREMENTED COUNTER
:15255 Q_D, ;UPDATE SRC ADDR FOR NEXT REFERENCE
:15256 R[R1]_LA+K[.4], ;CHECK ON BYTE OFFSET OF SRC ADDR
:15257 BEN/A[U1-O,
:15258 J/MOVCFCLUA
:15259
:15260 =*01 ;-----;D<1> VIA BEN/MUL, SC IS ZERO
:15261 MOVCFB:
:15262 R[R1]_LA+K[.1], ;-----;
:15263 J/MOVCRDBYTE
:15264
:15265 ;*11-----;
:15266 MOVCFWD:
:15267 R[R1]_LA+K[.2] ;UPDATE SRC ADDR TO REFLECT THIS READ
:15268
:15269 ;-----;
:15270 D[WORD]_CACHE, ;COPY DECREMENTED COUNTER
:15271 Q_D,
:15272 STATE_STATE.OR.K[.2],
:15273 J/MOVCFWRITE
:15274
:15275 ;-----;
:15276 MOVCRDBYTE:
:15277 D[BYTE]_CACHE,
:15278 Q_Q-K[.T],
:15279 C[K].UBCC,
:15280 STATE_STATE.OR.K[.1],
:15281 J/MOVCFWRITE
:15282
:15283 ; ****
:15284 ; * Patch no. 033, PCS 0A06 trapped to WCS 1165 *
:15285 ; ****
:15286
:15287 =0* ;-----;ALU <C>
:15288 MOVCFWD: ;DEST ON WORD (10) BOUNDARY
:15289 ;CHECK FOR AT LEAST 2 BYTES TO MOVE
:15290 D_Q-K[.2],
:15291 C[K].UBCC,
:15292 D(1)?,
:15293 J/MOVCFB ;D<1> VIA BEN/MUL
:15294
:15295 ;1*-----
:15296 D_Q-K[.2],
:15297 C[K].UBCC,
:15298 J/MOVCFWD
  
```

ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] Character string 14-Jan-82 B 16  
; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA OE, WCS124  
; CHAR .MIC [600,1204] Character string : MOV(3/5 MAIN LOOPS

Fiche 2 Frame B16 Sequence 402

Page 401

U 06CB, 0018,0024,0D80,F800,0284,6A08

:15299 ;SC = 0  
:15300 ;Q + ID[T2] = COUNT - 4  
:15301 ;ALU Z SET ON CURRENT CONTENTS OF Q  
:15302 ;LAB = CURRENT(UNALIGNED) SRC ADDR  
:15303 ;R1 = NEXT SRC ADDR(ALSO UNALIGNED), I.E LAB + 4  
:15304 ;D = CORRECT DATA FOR NEXT WRITE, I.E APPROPRIATELY ALIGNED  
:15305 ; BECAUSE OF 1 READ/LONG THAT WAS NOT AT BYTE 0 OFFSET  
:15306  
:15307 =1011 ;-----;ALU <1:0>  
:15308 MOVCFUA:  
:15309 VA\_LA.ANDNOT.K[.3], ;ALWAYS READ ALIGNED  
:15310 SC\_K[.3],  
:15311 J/MOVCFUA1  
:15312  
:15313 ;1111-----;  
:15314 MOVCFWRITE:  
:15315 LA\_RA[3], ;UPDATE LA ONLY  
:15316 VA\_LA,  
:15317 INTRPT\_STROBE, ;INTERRUPTS PENDING?  
:15318 FE\_SC, ;SAVE SC FOR A STATE OR SO  
:15319 STATE1-0?, ;HOW MANY BYTES TO WRITE?  
:15320 J/MOVCFWRITE  
:15321  
:15322 ==\*\*00 ;-----;STATE <1:0>  
:15323 MOVCFWRITE:  
:15324 CACHE\_D[LONG], ;4 BYTES TO WRITE  
:15325 R[R3]-LA+K[.4],  
:15326 BEN/INTERRUPT,  
:15327 J/MOVCFLP  
:15328  
:15329 ==\*\*01-----;1 BYTE TO WRITE  
:15330 CACHE\_D[BYTE],  
:15331 STATE\_STATE.ANDNOT.K[.1],  
:15332 ALU\_K[.1].SC\_ALU, ;SC\_1 FOR ADDR INCREMENTATION  
:15333 BEN/INTERRUPT,  
:15334 J/MOVCBWUPDATE  
:15335  
:15336 ==\*\*10-----;2 BYTES TO WRITE  
:15337 CACHE\_D[WORD],  
:15338 STATE\_STATE.ANDNOT.K[.2],  
:15339 ALU\_K[.2].SC\_ALU, ;SC\_2 FOR ADDR INCREMENTATION  
:15340 BEN/INTERRUPT,  
:15341 J/MOVCBWUPDATE  
:15342 =

U 06CF, 0000,173C,0180,F898,4300,0728

U 0728, 0018,0E14,1180,3298,0000,06B6

U 0729, 0018,8E38,0580,3000,1486,46F6

U 072A, 0018,4E38,0980,3000,1486,46F6

ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] Character string 14-Jan-82 Fiche 2 Frame C16 Sequence 403  
; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 JAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 402  
; CHAR .MIC [600,1204] Character string : MOV[3/5 MAIN LOOPS

C 16

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:15343      ;-----;
:15344      =110 ;-----; :INTERRUPTS?
:15345      MOVCBWUPDATE: ;-----;
:15346      R[R3]_LA+K[SC], ;-----;
:15347      D_ALU; ;-----;
:15348      SC_FE; ;-----; :GET BYTE OFFSET FOR BEN/MUL
:15349      Z?; ;-----; :RESTORE SC
:15350      J/MOVCFST ;-----; :ANY LEFT?
:15351
:15352      ;111-----;
:15353      R[R3]_LA+K[SC], ;-----; :THERE'S AN INTERRUPT PENDING
:15354      D_Q, ;-----; :RESTORE R3 AND PUT LOOPCOUNT IN D
:15355      J/MOVCPACKST ;-----; :GO PACK R0 AND HONOR INT.
:15356
:15357      =0* ;-----; :ALU <C>
:15358      MOVCFFILLMORE: ;-----;
:15359      Q_D+K[.2], ;-----; :Q_COUNT-4+2
:15360      STATE_STATE.OR.K[.2], ;-----;
:15361      CLK_UBCC, ;-----;
:15362      D(1)?; ;-----; :IS THERE 1 BYTE OR 1 LWD LEFT?
:15363      J/MOVCFILLBYTE ;-----;
:15364
:15365      ;1*-----;
:15366      MOVCFFILLWR: ;-----;
:15367      LA RA[5], ;-----; :PRESERVE LB WITH R1 FOR FAULTS + INTERRUPTS
:15368      D_LA, ;-----;
:15369      J/MOVCFWRITE ;-----;
:15370
:15371      =101 ;-----; :D<1> VIA BEN/MUL
:15372      MOVCFFILLBYTE: ;-----; :ONLY 1 BYTE LEFT
:15373      Q_Q+K[.1], ;-----; :Q_COUNT-2+1
:15374      CLK_UBCC, ;-----;
:15375      STATE_STATE-K[.1], ;-----; :CLEAR STATE <1> + SET STATE <0>
:15376      J/MOVCFILLWR ;-----;
:15377
:15378      ;111-----;
:15379      LA_RA[5], ;-----; :AT LEAST 1 WORD LEFT
:15380      D_LA, ;-----;
:15381      J/MOVCFWRITE ;-----; :GO MOVE 1 WORD

```

ZZ-ES0AA-124.0 ; CHAR .MIC [600,1204] Character string 14-Jan-82 D 16  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124  
 ; CHAR .MIC [600,1204] Character string : MOVC3/5 MAIN LOOPS

Fiche 2 Frame D16 Sequence 404  
 Page 403

U 0A08, 0043,0010,A080,F983,0084,661A

```
:15382 MOVCFLUA1:  

:15383     VA,VA+4,  

:15384     ALU 0+MAS1+1,  

:15385     RC[T0] ALU.RIGHT,SI/ASHR,  

:15386     SC K[.FFEO],  

:15387     J/MOVCFUNLRD  

:15388  

:15389 =0* -----;ALU <C>  

:15390 MOVCUNALMORE:  

:15391     VA_LA,  

:15392     SC_K[ZERO],  

:15393     D_Q,  

:15394     J7MOVCFWC  

:15395  

:15396 =1*-----;  

:15397 MOVCUNLRD:  

:15398     D[LONG]_CACHE,  

:15399     Q_D,  

:15400     LC RC[T0]&R1_LA+K[.4],  

:15401     BEN/ROR,  

:15402     J/MOVCFUNSHF
```

;PEPARE TO READ NEXT LWD ALIGNED  
;SC=3 SO CREATE FFFFFFF8,  
;SHIFT RIGHT TO GET FFFFFFFC (-4)  
;NEED -32 TO GET CORRECT DATA FROM  
;Q INTO D FOR NEXT WRITE

U 0618, 0C00,003C,1980,F800,0284,65C8

```
:15396  

:15397  

:15398  

:15399  

:15400  

:15401  

:15402  

:15403  

:15404  

:15405 =010 -----;  

:15406 MOVCUNSHF:  

:15407 =011 -----;LA = 01  

:15408     LA_RA[3],  

:15409     VA_LA,  

:15410     INTRPT_STROBE,  

:15411     D_DAL_SC, Q_D,  

:15412     SC_K[.18],  

:15413     J/MOVCFUNWRITE  

:15414  

:15415 =110-----;LA <1:0> = 10  

:15416     LA_RA[3],  

:15417     VA_LA,  

:15418     INTRPT_STROBE,  

:15419     D_DAL_SC, Q_D,  

:15420     SC_K[.10],  

:15421     J/MOVCFUNWRITE
```

;COPY PREVIOUS ALIGNED READ DATA  
;UPDATE FOR NEXT READ  
;CHECK LA<1:0>

U 061A, 0018,0214,11E0,4380,0000,0742

```
:15422  

:15423 =111-----;LA <1:0> = 11  

:15424     LA_RA[3],  

:15425     VA_LA,  

:15426     INTRPT_STROBE,  

:15427     D_DAL_SC, Q_D,  

:15428     SC_K[.8],  

:15429     J/MOVCFUNWRITE  

:15430 =  

:15431 -----;  

:15432 MOVC3/5WRITE:  

:15433     CACHE_D[LONG],  

:15434     R[R3]&LA+K[.4],  

:15435     BEN/INTERRUPT,  

:15436     J/MOVCFUNINT
```

;WRITE A LONGWORD ALIGNED  
;INCR DEST ADDR.  
;NOW BYTE 0 OF 'NEXT' LWD

U 0743, 0D00,003C,7DE0,F898,4284,6A09

U 0746, 0D00,003C,65E0,F898,4284,6A09

U 0747, 0D00,003C,01E0,F898,4284,6A09

U 0A09, 0018,0E14,1180,3298,0000,0726

ZZ-ESOAA-124.0 : CHAR .MIC [600,1204] .MICR02 1L(03) Character string 14-Jan-82 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 E 16 Fiche 2 Frame E16 Sequence 405 Page 404  
 : P1W124.MCR 600,1204] Character string : MOVC3/5 MAIN LOOPS

```

:15437 =110 ;-----;INTERRUPTS?
:15438 MOVCUNINT: ;NO INTERRUPTS PENDING
:15439 D_Q; ;D MOST RECENT L&D READ
:15440 Q_ID[T2]; ;LOAD COUNTER
:15441 LAB_R[R1]; ;LATCH SRC ADDR
:15442 VA_EA.AND.LC.; ;MASK OUT LOW BITS
:15443 Z?; ;MORE TO DO?
:15444 J/MOVCFUNMORE
:15445
:15446 ;111-----;
:15447 Q_ID[T2]; ;GET UN-INCREMENTED COUNTER
:15448 J7MOVCINTF
:15449
:15450 =0 ;-----;ALU <Z>
:15451 MOVCUNMORE: ;ANOTHER LWD LEFT TO DO?
:15452 RC[T2]_Q-K[.4]; ;MOST RECENT LWD READ
:15453 D_Q-K[.4];
:15454 Q_D;
:15455 CLK_LBCC;
:15456 VA_VA+4;
:15457 J/MOVCFUNOTHER
:15458
:15459 ;1-----;COUNT = 0
:15460 D NOT.R[R2], Q NOT.R[R2]; ;GET -(FILL COUNT) IN D AND Q LOW
:15461 STATE STATE.ANDNOT.K[.30];
:15462 BEN/STATE7-4;
:15463 J/MOVCMAYBEFILL
:15464
:15465 ;-----;
:15466 MOVCUNOTHER: ;SAVE DECREMENTED COUNTER
:15467 ID[T2]_D; ;RESTORE COUNTER(LC=-4)
:15468 Q_D-LC;
:15469 D_Q;
:15470 C31;
:15471 J/MOVCFUNMORE

```

U 0726, 0C10,0134,C9F0,2E08,0200,05BC

U 0727, 0000,003C,C9F0,2C00,0000,06B7

U 05BC, 0819,2000,11E0,F993,0010,040A

U 05BD, 0800,1628,79C0,F890,1404,47A3

U 040A, 0C11,0300,C9C0,3C00,0000,0618

ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] Character string 14-Jan-82 F 16 Fiche 2 Frame F16 Sequence 406  
 : P1W124.MCR 600,1204] MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 405  
 : CHAR .MIC [600,1204] Character string : MOVC3/5 BACKWARDS MOVE

```

:15472 .TOC   "      Character string      : MOVC3/5 BACKWARDS MOVE"
:15473
:15474 =00
:15475 MOVCBCKWD$MAYBE:
:15476     R[R5]_LC,
:15477     Q_LC,
:15478     CLK.UBCC,
:15479     C3?,
:15480     CALL,J/MOVCRBUMP
:15481
:15482
:15483 =10
:15484 MOVCRLP:
:15485     LAB_R1&RC[T2]_Q-K[.4].
:15486     D_Q-K[.4].          ;MORE TO DO
:15487     C[K.UBCC,
:15488     INTRPT.STROBE,
:15489     BEN/SC,             ;DECREMENT COUNTER
:15490     J/MOVCBCKSRC        ;SC > 0?
:15491
:15492 =11
:15493 EXITR: Q_R[R5],           ;ALL DONE
:15494     J/MOVCREADJUST       ;ALL DONE WITH SRC MOVE
:15495
:15496 =101
:15497 MOVCBCKSRC:
:15498     R[R1]&VA_LA-K[.4].    ;SC=0 - MOVE A LWD
:15499     SC_K[.4].            ;ASSUME IT'S A LWD
:15500     C3T?.                ;TEST IF 4 OR MORE BYTES LEFT
:15501     J/MOVCBCKSRC2
:15502
:15503 =111
:15504     R[R1]&VA_LA-K[.1].    ;DECREMENT SRC ADDR FOR 1 BYTE'S WORTH
:15505     SC_K[.1].            ;SET BYTE FLAG
:15506     J/MOVCRDBCK1
:15507
:15508 =0*
:15509 MOVCBCKSRC2:
:15510     R[R1]&VA_LA-K[.1].    ;A BYTE
:15511     SC_K[.1].            ;SET BYTE FLAG
:15512     J/MOVCRDBCK1
:15513
:15514 =1*
:15515     D[LONG]_CACHE.       ;A LWD
:15516     Q_D.                 ;READ A LWD
:15517     LA_RA[R3].            ;DUPLICATE COUNTER
:15518     STATE STATE.ANDNOT.K[.1]. ;LATCH DEST ADDR
:15519     BEN/INTERRUPT.        ;NOTE IT'S NOT A BYTE
:15520     J/MOVCBCKWRITE
  
```

U 0770, 0010,0339,01C0,FAA8,0010,05C4  
 U 0772, 0819,3400,1180,FB10,4010,0765  
 U 0773, 0000,003C,01C0,FA28,0000,06C4  
 U 0765, 0018,0300,1180,FA88,0284,661C  
 U 0767, 0018,0000,0580,FA88,0284,6A0C  
 U 061C, 0018,0000,0580,FA88,0284,6A0C  
 U 061E, 0000,0E3C,05E0,4098,1404,4786

ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] G 16  
 : P1W124,MCR 600,1204] MICR02 1L(03) Character string 14-Jan-82 Fiche 2 Frame G16 Sequence 407  
 : CHAR .MIC [600,1204] Character string 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 406

U 0726, 0018,1700,1D80,FA98,0282,05FC  
 U 0787, 000C,0038,0180,FB90,0000,0A11  
 U 05FC, 0000,013C,F180,3000,0084,4772  
 U 05FD, 0000,813C,F180,3000,0084,4772  
 U 0A0C, 0019,AE00,05C0,4098,1414,27B6

```

:15521 =110 ;-----;INTERRUPT?
:15522 MOVCBCKWRITE: ;-----;
:15523 R[R3]&VA_LA-K[SC]. ;DECREMENT DEST ADDR FOR BYTE OR LONG
:15524 SC ALU, ;PREPARE LO BIT FLAG
:15525 BEN/STATE3-0. ;BRANCH ON LWD OR BYTE
:15526 J/MOVCBCKWR1
:15527 ;-----;
:15528 ;111-----;INTERRUPT PENDING
:15529 LC RC[T2]&R1_LB.
:15530 J/MOVINTR
:15531 ;-----;
:15532 =***0 ;-----;STATE <3:1> NEVER SET
:15533 MOVCBCKWR1: ;-----;
:15534 CACHE_D[LONG]. ;-----;
:15535 SC_SC_ANDNOT,K[.FFFC]. ;PRESERVE BITS <1:0>
:15536 Z? ;MORE TO DO?
:15537 J/MOVCR LP
:15538 ;-----;
:15539 ;***1-----;BYTE WRITE
:15540 CACHE_D[BYTE]. ;-----;
:15541 SC_SC_ANDNOT,K[.FFFC]. ;-----;
:15542 Z? ;-----;
:15543 J/MOVCR LP
:15544 ;-----;
:15545 ;-----;
:15546 MOVCRDBCK1: ;-----;
:15547 D[BYTE] CACHE. ;READ 1 BYTE
:15548 LA RA[R3]. ;-----;
:15549 Q 0-K[.1]. ;DECREMENT COUNTER FOR 1 BYTE
:15550 CT.K.UBCC. ;-----;
:15551 STATE STATE,OR,K[.1]. ;NOTE IT'S A BYTE OPERATION
:15552 BEN/INTERRUPT.
:15553 J/MOVCBCKWRITE
:15554 ;-----;
:15555 ; ****
:15556 ; * Patch no. 032, PCS 0A0C trapped to WCS 1164 *
:15557 ; ****
  
```

ZZ-ES0AA-124.0 : CHAR .MIC [600,1204] Character string 14-Jan-82 H 16 Fiche 2 Frame H16 Sequence 408  
 : P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Page 407  
 ; CHAR .MIC [600,1204] Character string : MOVC3/5 BACKWARDS MOVE

```

:15558 : COME HERE WHEN MOVE LOOP EXHAUSTED - BEN ON STATE<6>
:15559 : TO TELL WHETHER TO FILL OR NOT.
:15560 : D AND Q HAVE -(FILL COUNT) IN BITS 15:0, AND THE COMPLEMENT
:15561 : OF 2 FILL CHARACTERS IN 31:16.
:15562 :
:15563 :=*011 -----;STATE <6>
:15564 MOVCMAYBEFILL:
:15565 :
:15566 :
:15567 :011 ;-----;
:15568 : PC&VA_PC, FLUSH_IB, ;NO FILL NECESSARY
:15569 : CLR.FPD, J/MOVCEXIT ;RESET IB (ONLY NECESSARY IF WE
:15570 : ; WERE RESTARTED) AND GO CLEAR REGS
:15571 :
:15572 R[R0]_Q.AND.K[.FFFF], ;USE THIS CODE UNTIL YOU
:15573 J/R245ZERO ;UNDERSTAND HOW THE IB WORKS.
:15574 :
:15575 :111-----;NEED TO FILL
:15576 R[R15]_0-Q, D_D.SWAP, SC_K[.10] ;NEED TO FILL. R2 HAD -(FILL CT)
:15577 ;IN <15:0>; NEGATE IT AND SET UP
:15578 ;TO REPLICATE FILLS FROM R2<31:16>
:15579 :
:15580 :
:15581 Q[R15].AND.K[.FFFF], ;CLEAR HI-ORDER CRUD FROM COUNT.
:15582 C[K.UBCC, D_DAL.SC] ;SET Z ON IT, PUT 4 FILLS IN D
:15583 :
:15584 :
:15585 R[R5]_NOT.D, ;STORE FILLS IN R5, CLEAR BIT 6
:15586 STATE_STATE-K[.20] ;(NEED TO FILL), SET BIT 5 (FILLING)
:15587 :
:15588 :
:15589 R[R2]_K[.FFFF], J/MOVCFPL ;SET UP R2 FOR NEXT EXIT. GO FILL.
:15590 ;(SC_NE_0 TO INDICATE FILLS)
:15591 :
:15592 :
:15593 :
:15594 :MOVCEXIT: ;THIS IS THE END.....
:15595 : R[R0]_Q.AND.K[.FFFF], ;SET R0 TO MAX(SRCLEN-DSTLEN,0)
:15596 : PC_PC+1,LOAD_IB ;START RELOADING INSTRUCTION BUFFER
:15597 :
:15598 R[R5]_0, D_0, Q_0, ;ZERO R5 AND PREPARE TO ZERO
:15599 J/MOVGETOUT ;R2 AND R4 AND EXIT VIA IRD.
  
```

ZZ-ES03A-124.0 ; CHAR .MIC [600,1204] I 16 Fiche 2 Frame I16 Sequence 409  
 ; P1W124.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA CE, WCS124 Page 408  
 ; CHAR .MIC [600,1204] Character string : MOV(C3/5, MOVTC, MOVTUC FPD)

```

;15600 .TOC   "      Character string      : MOV(C3/5, MOVTC, MOVTUC FPD"
;15601
;15602 ;THE FAULT VECTOR FOR MOV(C3/5 + MOVTC/TUC IS FORCED TO BE F80.
;15603
;15604 ;-----;
;15605 0F81: ;-----; ;WRITE FAULT ENTRY POINT
;15606     R[R3]_LA ;SAVE START-OF-ITERATION DSTADR
;15607
;15608 ;-----;
;15609 0F82: ;-----; ;READ FAULT ENTRY POINT
;15610 MOVC.RDFAULT: ;-----;
;15611     LC_RC[T2]&R1_LB, SD_NOT.SD ;SAVE START-OF-ITERATION SRCADR
;15612
;15613 ;-----; ;SET FAULT FLAG (IN SD), GET COUNT-4
;15614
;15615 MOVCINTR: ;-----; ;BACKWARDS MOVE INTERRUPT ENTRY
;15616     D_0+LC+1, ;CURRENT COUNT MINUS 4 IN RC[T2]
;15617     IR1? ;(MINUS 1 IF MOVTC OR MOVTUC)
;15618
;15619 =10 ;-----; ;IR <1>
;15620     D_D+K[.3] ;GET TRUE COUNT TO STORE IN R0
;15621
;15622 ;11-----;
;15623 MOVCPACKST: ;-----; ;COMMON ENTRY FOR REGISTER PACKING
;15624     D_D.SWAP, Q_PC, SC_K[ZERO], ;PUT LOOP COUNT IN D HIGH,
;15625     SS_SD, CLK_DBCC ;SS = FAULT FLG, CLR EALU.N & SC
;15626
;15627 ;-----;
;15628 =0* ;-----; ;CONSTRAINT BLOCK FOR CALL
;15629     R[RO]_D, ;SAVE LOOPCOUNT IN RO<31:16>
;15630     STATE_STATE.ANDNOT.K[.3], ;CLEAR STATE <1:0> SO IT CAN BE
;15631 ;-----; ;OR'D WITH PC DELTA VIA THE
;15632     CALL,J/BAKUP.PC ;BMUX USING THE PACK.FLOAT LEG.
;15633 ;-----; ;BAKUP.PC RETURNS PC DELTA IN D
;15634
;15635 ;1*-----;
;15636     EALU_STATE, ;FETCH, EFFECTIVELY, STATE <7:2>
;15637     R[RO]_D.OR.PACK.FP, ;COMBINE PC DELTA + STATE INTO
;15638     DT/WORD, SS? ;RO<15:0> AND CHK FAULT OR INT
;15639
;15640 =*1*0 ;-----; ;SIGN SRC(SS)
;15641     BEN/INTERRUPT, J/INTIO ;INTERRUPT - SEE WHICH KIND
;15642
;15643 ;***** * Patch no. 030, PCS 00F4 trapped to WCS 1162 *
;15644 ;***** *
;15645 ;***** *
;15646
;15647 ;*1*1-----;
;15648     J/FPD.RTN ;FAULT - TAKE THE EXCEPTION.
  
```

J 16

Character string 14-Jan-82      Fiche 2 Frame J16      Sequence 410  
 MICR02 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124      Page 409

ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] ; P1W124.MCR 600,1204]  
 ; CHAR .MIC [600,1204] Character string : MOVC3/5, MOVTC, MOVTUC FPD

:15649 ;MOVC/MOVTC/MOVTUC RESTART CODE - COME HERE FROM IRD IF FPD SET.  
 :15650  
 :15651 ;-----;  
 :15652 48:  
 :15653 MOVCRESTART:  
 :15654 LA RA[R0], :RO CONTAINS STATE + PC DELTA  
 :15655 D [A, :+ LOOPCOUNT BYTE-SWAPPED  
 :15656 STATE\_AMX.EXP :RESTORE STATE  
 :15657  
 :15658 :-----;  
 :15659 PC&VA\_D.OXT[BYTE]+PC, D.D.SWAP, :UPDATE PC AND UNSWAP LOOP COUNT  
 :15660 STATE\_STATE.ANDNOT.K[.F], :STATE BITS <3:0> NOT OF INTEREST  
 :15661 SC\_STATE.ANDNOT.K[.F] :SC GETS FLAG BITS FOR FWD MOVE  
 :15662  
 :15663 :-----;  
 :15664 Q\_D, D\_K[.1FO0].RIGHT :SAVE COUNT, GET FAULT VECTOR  
 :15665  
 :15666  
 :15667 ID[FPDA] D, D.Q.OXT[WORD], :ISOLATE LOOP CT IN WD, SET VECTOR  
 :15668 SS\_0&SD\_0, CLR.UBCC, :CLEAR FAULT FLAG AND SET Z ON CT  
 :15669 STATE7-4? :TEST MOV VS MOVT AND DIRECTION  
 :15670  
 :15671 =0110 :-----;STATE7-4  
 :15672 SC\_SC.ANDNOT.K[.50], Q\_D, :FWD MOVC - SET SC TO FILL FLAG  
 :15673 J/MOVCFLP  
 :15674  
 :15675 :0111-----;  
 :15676 SC\_R[R3].AND.K[.3], Q\_D, :BKWD MOVC - SC=DEST ADDR<1:0>  
 :15677 J/MOVCRLP  
 :15678  
 :15679 :1110-----;  
 :15680 D\_R[R2], ID[T0]\_D, Q\_0, :FWD MOVTC/TUC - GET FILL/ESC,  
 :15681 J7MOVTCFWD :SAVE COUNT AND RE-ENTER LOOP  
 :15682  
 :15683 :1111-----;  
 :15684 D\_R[R2], ID[T0]\_D, Q\_0, :BKWD MOVTC - GET FILL,  
 :15685 J7MOVTCBKWD :SAVE COUNT AND RE-ENTER LOOP

U 0048, 0800,003C,0180,F880,1408,6A12  
 U 0A12, 0817,8014,6180,F801,1684,4A14  
 U 0A14, 0858,0038,91E0,F800,0000,0A15  
 U 0A15, 0803,763C,B587,3C00,0010,06D6  
 U 06D6, 0000,003C,35E0,F800,0084,46B6  
 U 06D7, 0018,0034,0DE0,FA18,0082,0772  
 U 06DE, 0800,003C,C1F8,3E10,0000,032E  
 U 06DF, 0800,003C,C1F8,3E10,0000,032A

:15686 .TOC " Character string : SKPC, LOCC"  
:15687 :SKPC TIL UNEQUAL; LOCC TIL EQUAL  
:15688 :  
:15689 :  
:15690 :ALGORITHM:  
:15691 :THE SOURCE IS COMPARED WITH THE MASK CHARACTER TIL FOUND/NOT FOUND.  
:15692 :DEPENDING ON THE OP-CODE. THIS SEARCH IS CONDUCTED BY BYTES TIL A  
:15693 :LONGWORD BOUNDARY IS REACHED, AT WHICH TIME IT IS CONTINUED AS  
:15694 :LONGWORDS TIL < 4 BYTES REMAIN TO BE SEARCHED, WHEN IT REVERTS  
:15695 :TO BYTE-WISE SEARCH AGAIN.  
:15696 :  
:15697 :INPUTS:  
:15698 :Q CHARACTER FOR THE COMPARISON(1ST OPERAND)  
:15699 :D NUMBER OF BYTES TO COMPARE(2ND OPERAND)  
:15700 :  
:15701 :REGISTER USAGE:  
:15702 :R0 BYTE 1-0 = SRC LEN  
:15703 :BYTE 2 = PC DELTA FOR FPD  
:15704 :BYTE 3 = COMP CHAR FOR FPD  
:15705 :R1 SRC ADDR  
:15706 :Q LENGTH  
:15707 :RC 2 COMPARE CHAR  
:15708 :  
:15709 :OUTPUTS:  
:15710 :R0 NUMBER OF BYTES REMAINING IF BYTE LOCATED OR 0 IF NOT LOCATED  
:15711 :R1 ADDRESS OF BYTE LOCATED + 1 OR END OF STRING + 1  
:15712 :  
:15713 :LABELS OF INTEREST:  
:15714 :SKPRES1 RESUME EXECUTION AFTER RECOVERING FROM AN INTERRUPT/EXCEPTION  
:15715 :SKPBYTES READ + COMPARE BY BYTES LOOP  
:15716 :SKPALIGNED START OF LWD COMPARES. MAKE A LWD OF COMPARE CHAR  
:15717 :SKPLONGLOOP READ + COMPARE BY LWDS LOOP

ZZ-ESOAA-124.0 ; CHAR .MIC [600,1204] .MIC [600,1204] Character string 14-Jan-82 L 16  
 : P1WT24.MCR 600,1204] MICRO2 1L(03) 14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124 Sequence 412  
 : CHAR .MIC [600,1204] Character string : SKPC, LOCC Page 411

	:15718	488:	-----;	
U 0488, 0019,2035,4980,F990,0000,047E	:15719	R[C72] Q.AND.K[.FF],	;1ST ARG IS COMPARE BYTE	
	:15720	CALL,J7ASPC	;GET 3RD ARG	
	:15721			
U 04E8, 0019,2034,C180,FA80,0000,02B8	:15722	4E8:	-----;	
	:15723	R[R0]_Q.AND.K[.FFFF]	;2ND ARG IS LENGTH	
	:15724			
U 02B8, 0001,003D,3DF0,2E88,0000,09E4	:15725	=0****00 -----;	:RETURN40 + RETURN2	
	:15726	R[R1] D,	;ARG 3 IS ADDR	
	:15727	Q_IDEP[SL],	;PREPARE TO CLEAR PSL CC	
	:15728	CALL,J/CLRPSLCC	;	
	:15729			
U 02F8, 0818,0035,C180,FA00,0010,0E16	:15730	=1****00 -----;	:RETURN2 NEEDED	
	:15731	SKPRES1:	;FPD RESTART LOCATION	
	:15732	CALL,J/SETFPD,	;SET FPD BIT	
	:15733	D_R[R0].AND.K[.FFFF],	;GUARANTEE IT'S A WORD FOR RESTART ALSO	
	:15734	C[K].UBCC	;CHECK ON SRC LENGTH	
U 02F9, 0000,003C,0180,F800,0000,0A26	:15735			
	:15736			
	:15737	J/SKPFPD	;SKPC/LOCC FPD ADDR	
	:15738			
U 02FA, 0000,003C,0180,F800,0000,0A26	:15739			
	:15740	J/SKPFPD	;SKPC/LOCC FPD ADDR	
	:15741			
	:15742			
U 02FB, 0000,013C,01E0,FA08,0200,060C	:15743	Z?.	;BRANCH ON LENGTH > 0.	
	:15744	Q_D,	;COPY LENGTH	
	:15745	VA_R[R1]	;LOAD ADDR OF 1ST BYTE	

I	1	I-stream decode forks	:	A-FORK	for VAX Instructions
C	1	I-stream decode forks	:	A-FORK	for VAX Instructions
D	1	I-stream decode forks	:	B-FORK	for VAX Instructions
E	1	I-stream decode forks	:	B-FORK	for VAX Instructions
F	1	I-stream decode forks	:	B-FORK	for VAX Instructions
G	1	I-stream decode forks	:	B-FORK	for VAX Instructions
H	1	I-stream decode forks	:	B-FORK	for VAX Instructions
I	1	I-stream decode forks	:	B-FORK	fcr VAX Instructions
J	1	I-stream decode forks	:	B-FORK	for VAX Instructions
K	1	I-stream decode forks	:	B-FORK	for VAX Instructions
L	1	I-stream decode forks	:	B-FORK	for VAX Instructions
M	1	I-stream decode forks	:	B-FORK	for VAX Instructions
N	1	I-stream decode forks	:	B-FORK	for VAX Instructions
B	2	I-stream decode forks	:	B-FORK	for VAX Instructions
C	2	I-stream decode forks	:	B-FORK	for VAX Instructions
D	2	I-stream decode forks	:	B-FORK	for VAX Instructions
E	2	I-stream decode forks	:	B-FORK	for VAX Instructions
F	2	I-stream decode forks	:	B-FORK	for VAX Instructions
G	2	I-stream decode forks	:	B-FORK	for VAX Instructions
H	2	I-stream decode forks	:	B-FORK	for VAX Instructions
I	2	I-stream decode forks	:	C-FORK	for VAX Instructions
J	2	I-stream decode forks	:	C-FORK	for VAX Instructions
K	2	I-stream decode forks	:	C-FORK	for VAX Instructions
L	2	I-stream decode forks	:	C-FORK	for VAX Instructions
M	2	I-stream decode forks	:	C-FORK	for VAX Instructions
N	2	I-stream decode forks	:	C-FORK	for VAX instructions
B	3	I-stream decode forks	:	C-FORK	for VAX Instructions
C	3	I-stream decode forks	:	C-FORK	for VAX Instructions
D	3	I-stream decode forks	:	C-FORK	for VAX Instructions
E	3	I-stream decode forks	:	C-FORK	for VAX Instructions
F	3	I-stream decode forks	:	C-FORK	for VAX Instructions
G	3	I-stream decode forks	:	C-FORK	for VAX Instructions
H	3	I-stream decode forks	:	C-FORK	for VAX Instructions
I	3	I-stream decode forks	:	C-FORK	for VAX Instructions
J	3	I-stream decode forks	:	C-FORK	for VAX Instructions
K	3	I-stream decode forks	:	C-FORK	Specifier Evaluation Subroutine
L	3	I-stream decode forks	:	C-FORK	Specifier Evaluation Subroutine
M	3	I-stream decode forks	:	C-FORK	Specifier Evaluation Subroutine
N	3	I-stream decode forks	:	C-FORK	Specifier Evaluation Subroutine
B	4	I-stream decode forks	:	C-FORK	Specifier Evaluation Subroutine
C	4	I-stream decode forks	:	C-FORK	Specifier Evaluation Subroutine
D	4	ARITH.MIC	:		
E	4	Integer arithmetic	:	Multiplication subroutine	
F	4	Integer arithmetic	:	Multiplication subroutine	
G	4	Integer arithmetic	:	Divide subroutine	
H	4	Integer arithmetic	:	MULB2, MULB3, MULW2, MULW3, MULL2, M	
I	4	Integer arithmetic	:	MULB2, MULB3, MULW2, MULW3, MULL2, M	
J	4	Integer arithmetic	:	MULB2, MULB3, MULW2, MULW3, MULL2, M	
K	4	Integer arithmetic	:	MULB2, MULB3, MULW2, MULW3, MULL2, M	
L	4	Integer arithmetic	:	EMUL	
M	4	Integer arithmetic	:	EMUL	
N	4	Integer arithmetic	:	EMUL	
B	5	Integer arithmetic	:	DIVB2, DIVB3, DIVW2, DIVW3, DIVL2, D	
C	5	Integer arithmetic	:	DIVB2, DIVB3, DIVW2, DIVW3, DIVL2, D	
D	5	Integer arithmetic	:	DIVB2, DIVB3, DIVW2, DIVW3, DIVL2, D	
E	5	Integer arithmetic	:	DIVB2, DIVB3, DIVW2, DIVW3, DIVL2, D	
F	5	Integer arithmetic	:	EDIV	
G	5	Integer arithmetic	:	EDIV	
H	5	Integer arithmetic	:	EDIV	
I	5	INDEX.MIC	:		

J	Index	instruction	:	INDEX
K	Index	instruction	:	INDEX
L	Index	instruction	:	INDEX
M	FLOAT.MIC		:	
N	F & D	floating point	:	CMPF
B	F & D	floating point	:	CMPF
C	F & D	floating point	:	ADDF, SUBF
D	F & D	floating point	:	ADDF, SUBF
E	F & D	floating point	:	ADDF, SUBF
F	F & D	floating point	:	ADDF, SUBF
G	F & D	floating point	:	ADDF, SUBF
H	F & D	floating point	:	ADDF/SUBF ROUTINE
I	F & D	floating point	:	ADDF/SUBF ROUTINE
J	F & D	floating point	:	ADDF/SUBF ROUTINE
K	F & D	floating point	:	ADDF/SUBF ROUTINE
L	F & D	floating point	:	MULF
M	F & D	floating point	:	MULF
N	F & D	floating point	:	MULF
B	F & D	floating point	:	DIVF
C	F & D	floating point	:	DIVF
D	F & D	floating point	:	DIVF
E	F & D	floating point	:	CMPD
F	F & D	floating point	:	CMPD
G	F & D	floating point	:	UNPACK DOUBLE OPERANDS
H	F & D	floating point	:	UNPACK DOUBLE OPERANDS
I	F & D	floating point	:	UNPACK DOUBLE OPERANDS
J	F & D	floating point	:	UNPACK DOUBLE OPERANDS
K	F & D	floating point	:	PACK DOUBLE RESULT
L	F & D	floating point	:	PACK DOUBLE RESULT
M	F & D	floating point	:	ADDD, SUBD
N	F & D	floating point	:	ADDD, SU3D
B	F & D	floating point	:	ADDD, SUBD
C	F & D	floating point	:	ADDD, SUBD
D	F & D	floating point	:	ADDD, SUBD
E	F & D	floating point	:	ADDD, SUBD
F	F & D	floating point	:	ADDD, SUBD
G	F & D	floating point	:	ADDD, SUBD
H	F & D	floating point	:	ADDD, SUBD
I	F & D	floating point	:	ADDD, SUBD
J	F & D	floating point	:	ADDD, SUBD
K	F & D	floating point	:	MULD
L	F & D	floating point	:	DIVD
M	F & D	floating point	:	DIVD
N	F & D	floating point	:	DIVD
B	F & D	floating point	:	DIVD
C	F & D	floating point	:	DIVD
D	F & D	floating point	:	UNPACK ONE DOUBLE OPERAND
E	F & D	floating point	:	CVTBF, CVTWF, CVTLF
F	F & D	floating point	:	CVTBF, CVTWF, CVTLF
G	F & D	floating point	:	CVTBD, CVTWD, CVTLD
H	F & D	floating point	:	CVTFD, CVTDF
I	F & D	floating point	:	CVTFD, CVTDF
J	F & D	floating point	:	CVTFB, CVTFW, CVTFL, CVTRFL
K	F & D	floating point	:	CVTDB, CVTDW, CVTDL, CVTRDL
L	F & D	floating point	:	CVTDB, CVTDW, CVTDL, CVTRDL
M	F & D	floating point	:	CONVERT FLOATING TO INTEGER
N	F & D	floating point	:	CONVERT FLOATING TO INTEGER
B	F & D	floating point	:	CONVERT FLOATING TO INTEGER
C	F & D	floating point	:	CONVERT FLOATING TO INTEGER
D	F & D	floating point	:	ACBF

E 10	F & D floating point	: ACBF	M 14	Field instructions	: INSV
F 10	F & D floating point	: ACBF	N 14	Field instructions	: INSV
G 10	F & D floating point	: ACBF	B 15	Field instructions	: INSV
H 10	F & D floating point	: ACBF	C 15	CHAR.MI	
I 10	F & D floating point	: ACBD	D 15	Character string	: Utilities
J 10	F & D floating point	: ACBD	E 15	Character string	: Utilities
K 10	F & D floating point	: ACBD	F 15	Character string	: Utilities
L 10	F & D floating point	: MULD	G 15	Character string	: MOVC3, MOVC5
M 10	F & D floating point	: MULD	H 15	Character string	: MOVC3/5 INITIALIZATION
N 10	F & D floating point	: MULD	I 15	Character string	: MOVC3/5 INITIALIZATION
B 11	F & D floating point	: MULD	J 15	Character string	: MOVC3/5 INITIALIZATION
C 11	F & D floating point	: MULD	K 15	Character string	: MOVC3/5 INITIALIZATION
U 11	F & D floating point	: EMODF	L 15	Character string	: MOVC3/5 MAIN LOOPS
E 11	F & D floating point	: EMODF	M 15	Character string	: MOVC3/5 MAIN LOOPS
F 11	F & D floating point	: EMODF	N 15	Character string	: MOVC3/5 MAIN LOOPS
G 11	F & D floating point	: EMODF	B 16	Character string	: MOVC3/5 MAIN LOOPS
H 11	F & D floating point	: EMODF	C 16	Character string	: MOVC3/5 MAIN LOOPS
I 11	F & D floating point	: EMODF	D 16	Character string	: MOVC3/5 MAIN LOOPS
J 11	F & D floating point	: EMODD	E 16	Character string	: MOVC3/5 MAIN LOOPS
K 11	F & D floating point	: EMODD	F 16	Character string	: MOVC3/5 BACKWARDS MOVE
L 11	F & D floating point	: EMODD	G 16	Character string	: MOVC3/5 BACKWARDS MOVE
M 11	F & D floating point	: POLYF	H 16	Character string	: MOVC3/5 BACKWARDS MOVE
N 11	F & D floating point	: POLYF	I 16	Character string	: MOVC3/5, MOVTC, MOVTUC FPD
B 12	F & D floating point	: POLYF	J 16	Character string	: MOVC3/5, MOVTC, MOVTUC FPD
C 12	F & D floating point	: POLYF	K 16	Character string	: SKPC, LOCC
D 12	F & D floating point	: POLYF	L 16	Character string	: SKPC, LOCC
E 12	F & D floating point	: POLYF			
F 12	F & D floating point	: POLYF			
G 12	F & D floating point	: POLYF			
H 12	F & D floating point	: POLYD			
I 12	F & D floating point	: POLYD			
J 12	F & D floating point	: POLYD			
K 12	F & D floating point	: POLYD			
L 12	F & D floating point	: POLYD			
M 12	F & D floating point	: POLYD			
N 12	F & D floating point	: POLYD			
B 13	F & D floating point	: POLYD			
C 13	F & D floating point	: POLYD			
D 13	F & D floating point	: POLYD			
E 13	INIT2.MIC				
F 13	Initialize microcode	: INITIALIZE MACHINE ROUTINE			
G 13	Initialize microcode	: INITIALIZE MACHINE ROUTINE			
H 13	Initialize microcode	: INITIALIZE MACHINE ROUTINE			
I 13	Initialize microcode	: INITIALIZE MACHINE ROUTINE			
J 13	Initialize microcode	: INITIALIZE MACHINE ROUTINE			
K 13	ASPC.MIC				
L 13	I-stream decode forks	: Address Specifier Evaluation			
M 13	I-stream decode forks	: Address Specifier Evaluation			
N 13	I-stream decode forks	: Address Specifier Evaluation			
B 14	I-stream decode forks	: Address Specifier Evaluation			
C 14	I-stream decode forks	: Address Specifier Evaluation			
D 14	FIELD.MIC				
E 14	Field instructions	: FFS, FFC, CMPV, CMPZV, EXTV, EXTZV			
F 14	Field instructions	: FFS, FFC, CMPV, CMPZV, EXTV, EXTZV			
G 14	Field instructions	: FFS, FFC, CMPV, CMPZV, EXTV, EXTZV			
H 14	Field instructions	: FFS, FFC, CMPV, CMPZV, EXTV, EXTZV			
I 14	Field instructions	: FFS, FFC, CMPV, CMPZV, EXTV, EXTZV			
J 14	Field instructions	: INSV			
K 14	Field instructions	: INSV			
L 14	Field instructions	: INSV			